Free Open Source Software Stacks and **Open Hardware Technologies: Revolutionizing the World** by: Tassadaq Hussain **Professor Department of Electrical Engineering Director Centre for AI and BigData Namal University Mianwali Collaborations: Barcelona Supercomputing Center, Spain European Network on High Performance and Embedded Architecture and Compilation Pakistan Supercomputing Center**



Trainer and Centre Introduction

- Past Present and Future of AI and Big Data
- Addressing Challenges with Open Source Software and Hardware Technologies
- Namal Centre for Al and BigData: Strength and Achievements

Introduction

Education:

PhD. Barcelona-Tech Microsoft Research, Infineon Technologies France, Microsoft Research Cambridge, IBM

Suspenseful record of academic management as Professor and Dean

Enhanced Education Quality by Inculcating Outcome Based Education by Applied and Sustainable Projects

Experience:

19+ year's versatile experience in the area of Computer Architecture, AI, Software Architecture, Big-Data Architecture Served National and International Academia, Industry and Government

- Barcelona Science Park Spain
- Cambridge Science Park UK
- Technopolis Of Sofia-Antipolis, France





WWW.Tassadaq.PakistanSupercomputing.COM

Innovation, Research and Commercialization



Innovation and Research

• 110+ Million Pkr National and Int²l Funding.

Supercomputing and Artificial Intelligence Smart Electric Motor Controllers Biomedical Applications

- 80+ Publications
- 10 Patents
- 10 MVPs
- 5 Int'l Collaborations





• Development & Commercialization

60+ Million of Industrial Investments.

Developed Digital Systems for Industry. Transform Idea into product. Innovation and Commercialization for Sustainable economic and industrial development.

• Capacity Building:

Conducted more than 50 national and international workshops and training on Commercializable research, Writing successful grant proposal, and research and innovation.

Provides Consultancy and Support for Entrepreneurship, Start-ups, Business Innovation and Technology transfer.









Int'l Projects

 Design Ultra Low Cost Display Camera Interface for Mobile Baseband XGold Chip (Infineon Techonogies, 200 million single chip)





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- Implementation of Reverse Time Migration on FPGAs (BSC-REPSOL, PLDA Italia, Cambridge Science Park)





Int'l Projects

 Design Ultra Low Cost Display Camera Interface for Mobile Baseband XGold Chip (Infineon Techonogies, 200 million single chip)



- Implementation of Reverse Time Migration on FPGAs (BSC-REPSOL, PLDA Italia, Cambridge Science Park)
- Open source European full-stack ecosystem based on a new RISC-V CPU (Barcelona Supercomputing Center)



Current Challenge and Sustainable and Scalable Solutions

- World Data Size = 170 Zettabytes, doubling every 18 months.
- To handle big-data, **AI algorithms** are the only solution.
- The computational demands of AI algorithms are experiencing exponential growth.
 (ExaFLOPS/Day)
- Supercomputing is the only solution to store big-data and process the AI.

Secure



Indigenous Commercializable Industrial Development Well being

Centre for AI and BigData

Vision:

Solve local compute-intensive problems using smart solutions and high-performance technologies.

Mission

To provide indigenous digital solutions for multi-disciplinary local problems.

Acquire analog data, digitize, store it and propose a technological solution for analysis, classification, prediction, control and simulation.





Targets

- a) Specialized Training
- b) Linkages and Collaborations
- c) Research and Publications
- d) Innovation and Prototype
- e) Fund Grant Hunting
- g) Services and Consultancy
- h) Technology Transfer
- i) Revenue Generated

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Mankind Progress



From Age of Empirical Science to Data-Science



Global Data Creation is About to Explode

Actual and forecast amount of data created worldwide 2010-2035 (in zettabytes)



BigData and AI Algorithms

Performance

- Execution Time
- Accuracy "The accuracy of the model is inherently tied to the quality, diversity, and representativeness of the data used for training and evaluation."
- Scalability "Methods that scale with computation are the future of Artificial Intelligence" — Rich Sutton,



Computation Demand

Petaflop/s-days



The total amount of compute, in petaflop/s-days,[2] used to train selected results that are relatively well known, used a lot of compute for their time, and gave enough information to estimate the compute used.



Deep and steep

Computing power used in training AI systems Days spent calculating at one petaflop per second*, log scale



Al Algorithms and Intellectuality: By Enhancing Computational Capability ?



Compute Vs Intellectual Capability



Al Computational Requirements



https://towardsdatascience.com/artificial-intelligence-is-a-supercomputing-problem-4b0edbc2888d



Ecosystem of Modern Industry



Open source tools democratizing the world

- GCC has revolutionized the software industry.
- Linux has **revolutionized** computing industry.
- AI models have **revolutionized** intelligent computing.
 - Open-source AI Frameworks
 - Open-source Data-source
 - Open-source AI Models



Al and Specialized Accelerators Performance Gap





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Computing Architectures to Solve AI Problems

- Smart Sensors
- Processor in Memory (PIM)
- Processing-in-Storage
- Processor in NIC (Network Interface Card)
- Compute-in-Edge Devices
- Brain Inspired Computers





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Democratization in Microelectronics

- GCC has revolutionized the Software Industry.
- Linux has revolutionized Computing Industry.
- AI models have **revolutionized** Intelligent Computing.
- Open Hardware is **revolutionizing** the Secure Computing.
- Open Silicon is next => Indigenous Development.

The Power of Open Source: Innovation, Flexibility, and Security

- **Research and Innovation**
- **Customization and Flexibility**
- **Reducing Costs**
- **Accelerating Development**
- **Community Collaborations**
- Transparency and Trustworthiness
- **Reduced Dependence on Proprietary Solutions**
- Secure and Trusted Execution

Open Source Tool for Hardware Development



SkyWater PDK (Process Design Kit), in collaboration with organizations like eFabless

Hardware Design Going to Follow Journey of Software Design

Open-Source	Software	Hardware
High-Level Languages	Python, Ruby, R, Javascript, Julia	Chisel, PyMTL, PyRTL, Myhdl, JHDL, Cλash, Calyx, Dfiant
Libraries	C++ Stl, Python Std Libs	Basejump
Tool Chains	GCC, LLVM, CPython, MRI, PyPy, V8	Icarus Verilog, Verilator, Qflow, Yosys, Timberwolf, Qrouter, Magic, Klayout, Ngspice
Standards	POSIX	RISC-V ISA, ROCC, Tilelink
Systems	Linux, Apache, Mysql, Memcached	RocketChip, Pulp/Ariane, OpenPiton, ChipYard, BOOM, FabScalar, MIAOW, Nyuzi
Methodologies	Agile Software Design	Agile Hardware Design
Cloud	IaaS, Elastic Computing	IaaS, Elastic Cad

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Sensors Netowrk, IoT, Automation

Fields, Farms, Processing Units and

Research Labs



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Real Time Computing Decision Support System





User Access Baremetal: ssh namal-hpc@10.0.0.154 Cloud Application: http://10.0.0.153:8501/

Centre for AI and BigData

 OpenSource Full-Stack Ecosystem for Secure Digital Systems







Supercomputing for AI and BigData Applications



OpenSource Full-Stack Ecosystem for Secure Processor Architecture

Hardware Architecture

- Low Power and Low Cost Digital System
- Uni/Multi Core System on a Chip
- Single Board Computer
 - Hardware Software Co-Design
 - High Performance Computing
- Intelligent and Real-time Applications
 - Industrial Automation
 - Machine Learning



Digital System Design Flow

Diagramming AAAAAA Simulation and Emulation **Digital System Design** System Integration **Functional Verification Formal Verification Timing Analysis FPGA** Prototyping \succ **Physical Design**

Diagramming Micro-Architecture



Simulation and Emulation

Spike: Functional, instruction-level accurate simulator for RISC-V ISA.

- QEMU: Functional simulator with instruction-level accuracy for various architectures.
- Gem5: Cycle-level accurate simulator for modeling detailed microarchitecture and system performance.



Digital System Design

- Switch Level
- Gate Level
- Register Transfer Level
- System / High Level

System Integration (SoC)

FuseSoC: A hardware IP management tool and build system that simplifies the integration of reusable IP blocks and automates the FPGA and ASIC build processes..

OpenPiton: A scalable, open-source manycore processor framework that can be integrated into custom research and industrial applications.

LiteX: A flexible and efficient framework for creating SoC designs using open-source hardware IPs and toolchains, with support for a variety of FPGAs and CPUs.



Functional Verification

Cocotb (Cocotestbench): A coroutinebased Python testbench framework for verifying HDL designs using high-level, Python-driven simulations.

SVUnit: A SystemVerilog unit testing framework designed for functional verification of hardware designs through automated test generation and execution.

Formal Verification, Physical Design and Timing Analysis:

SymbiYosys (Sby) integrates with backend tools such as Yosys and SMT solvers to formally verify properties like safety and liveness in hardware circuits. It helps to ensure correctness by exhaustively checking the design against specified constraints.

OpenSTA and OpenTimer for Timing Analysis.

Physical Design: OpenRoad, QFlow, Yosys, and Magic

Supercomputing Platform for AI and BigData Applications

Bare-Metal and Containerized Cluster Infrastructure:

Distributed Hardware Interfacing, Network Configuration and Distributed Computing Software Deployment

Data Center and Cloud Infrastructure:

- Storage systems, networking equipment, and software configuration
- Al Applications for Scientific and Engineering Problems
 - Distributed AI applications for multi-node bare-metal system
- HPC Application Parallel Programming
 - Heterogeneous multi-node parallel processing using parallel programming models







Supercomputing Platform with 20 Servers Compute Nodes

- Each node having:
 - Two XEON processors Intel(R) E5-2673 v4, 128 GB Main Memory
 - NVIDIA GPUs Ada Architecture 24GDDR
- Storage: 50 TByte SSD
- Linux Operating system
- Interconnection Fast Ethernet
- Open Source Software stack
 - Cloud, Baremetal and Embedded System
 - Parallel Programming and Scientific Computing
 - Chip Design
 - Distributed Artificial Intelligence
- Application Development
 - Digital System and VLSI Design
 - Parallel Processing, AI and BigData
 - IoT, Edge Computing
 - Modeling and Simulations



Developing Supercomputing for Al

(тм)

PAKISTAN SUPERCOMPUTING





(Up To 500 TFLOPS)

Cluster 5 Server Node (Up To 76 TFLOPS) Infini Band

Chip

4 cores



Server Node (upto 20 TFLOPS): 48 cores 96 GB RAM 1 TB Disk 2 GPUs **Ce**

CentOS Linux



Barcelona Supercomputing Center Centro Nacional de Supercomputación



AI Model Parallelism

Model Parallelism

Different layers of the network distributed across different devices

Data Parallelism

Same model in every one of the GPUs, each processing a separate piece of the data, a separate portion of the mini-batch.



DATA PARALLELISM



Achievement

Bare-metal Cluster

- 1 Peta FLOPS
 - Chip Design FOSSS RTL-GDS

Cloud Applications

- Agri-Rice Classification (Online Application Industrial Partner Alkaram Rice)
- Live Stock Breed Identification (Application Punjab LiveStock)
- Soil Analysis (Completed App)
- Foot Analytic for Rehabilitation (Startup)

Digital Systems

- FPGA based Computer Vision System for Rice Color Sorting (Funding Secured)
- BLDC Motor Controller

Sept 2023 – June 2024

- a) Specialized Training
- 4 Schools and Workshop
- 20 Talks
- b) Linkages and Collaborations 50+ Organizations
- c) Research and Publications
- 1 I.F. Journal
- 3 Conference Paper
- d) Innovation and Prototype
- 4 MVP
- 6 FYPs (Cloud Applications)
- f) Fund Grant Hunting
- Submitted 24 Million PKR
- g) Services and Consultancy
- h) Technology Transfer
- i) Revenue Generated
- 1.5 Million PKR

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