Industry Status of RISC-V SW Ecosystem

Part of the RISC-V labs Initiative

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Presenter

Ali Tariq

- BSc. Electrical Engineering - Computer
- Background in
  - Power Electronics
  - Embedded Systems Engineering
  - RTL Design and verification
  - Linux System Administration
- Currently working on DevOps, Automation, building Cloud Computing infrastructure for RISC-V software development and contributor in open-source community

10x ENGINEERS

10xEngineers.ai

The only **design & verification** services company focusing **exclusively** on

RISC-V & Image Signal Processors

Founded in 2021, led by industry veterans, the team has **70+ highly-skilled engineers** and rapidly growing

Working with **6 clients** in datacenter, 5G, automotive and AI-on-the-edge domain

Our customers have shortened the time-to-market and **reduced cost by 30%**

We are a **RISC-V Development Partner**, contributors in ratification of RISC-V ISA

Since 2020, our team has been **working with leading RISC-V** vendors in the world

One of the leading commercial **contributor to RV OS cores** (like CVA6) and accelerators (RVV Ara)

Front-end Design

- RTL design (SV & Chisel)
- Synthesis, DFT, STA
- FPGA Implementation

Design Verification

- Tesplan dev & execution
- UVM testbench development
- Coverage Closure
- Random Test Generators
- Architecture Compatibility Testing

Compilers & Toolchains

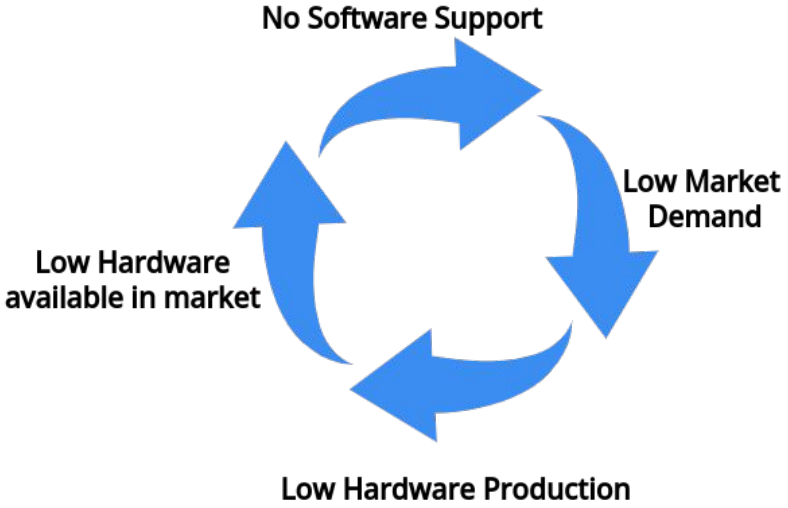
- **LLVM** development
- Creating & C intrinsics
- **MLIR** to RV lowering
- Automation & CI/CD
- RISC-V QEMU Setup

3. Why SW support is important

- Users tend to buy computers which have optimized software with good computing power
- Software organizations port their software on computers which already have some tooling support available

3. Why SW support is important

Software Developers Tend to develop software for architectures which have considerable market or user demand



Without software support, application class processor is of no use!

3. Why SW support is important

Discontinued architectures due to no SW support

- DEC Alpha
- IA-64
- SPARC
- Transmeta Crusoe

4. Hurdles in RISC-V SW Ecosystem

A. Why RISC-V SW support is lagging

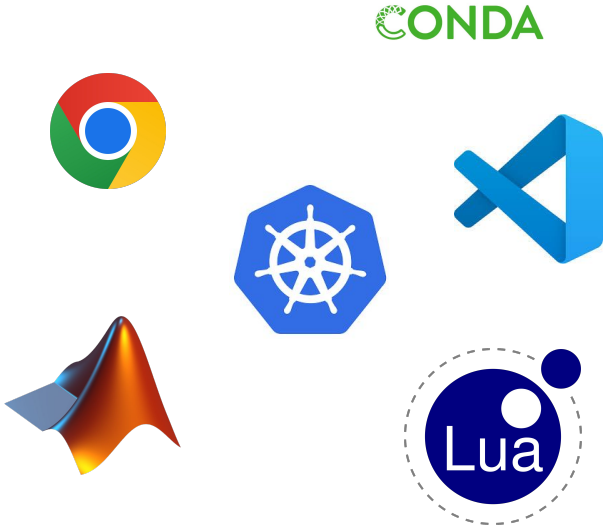
- Emphasis on development of hardware design and extensions
- Hardware usually not available in time
- Available hardware is not up to date with specifications (due to fabrication process and PD verification)
- Market Demand is limited to developers at present - low motivation of big organizations to port software to RISC-V

4. Hurdles in RISC-V SW Ecosystem

B. Which software are not yet ported (Non-Exhaustive List)

- Open-source
  - Kubernetes
  - Conda/miniconda
  - Nvim
  - .Net/C#

- Proprietary
  - MATLAB
  - Microsoft VScode
  - Google Chrome



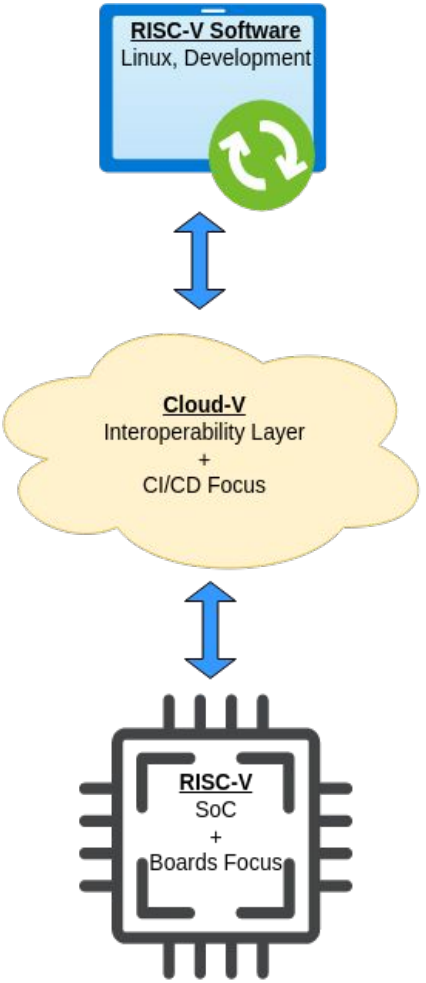
5. RISC-V initiatives for SW development

- RISC-V International has several subgroups (https://lists.riscv.org/g/main/subgroups)
- Lab Partners is a subgroup of RISC-V international for giving remote access to users around the world
  - Eliminates need to wait and buy RISC-V hardware for software development

6. What is Cloud-V

Cloud-V is a platform for testing **RISC-V** applications on **RISC-V instances** in the **cloud.**

- Includes emulated and hardware compute instances
- Includes all the tooling necessary for application development



6. What is Cloud-V

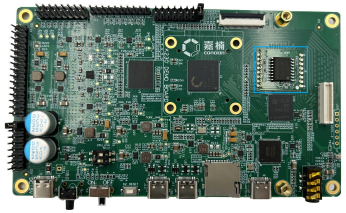
A. Emulated vs Physical Hardware RISC-V instances

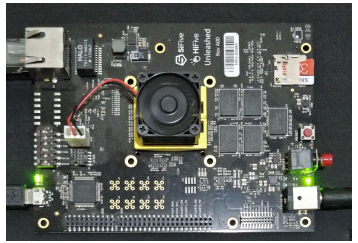
HW Instance	**Emulated Instance**
Lags behind the current specification	Stays up to date with current specification
Good for board-specific testing and development	Need to create an emulator model for it first
Max computing power is limited to hardware specification	Max computing power can be increased based on the host computing power

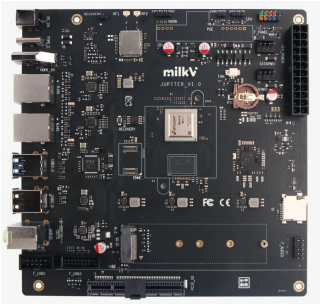
6. What is Cloud-V

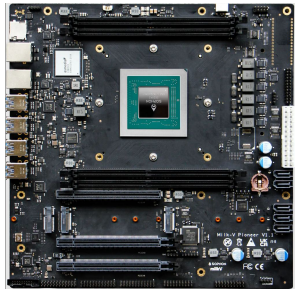
RISC-V Hardware

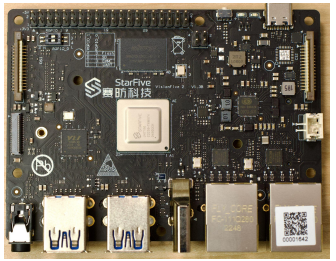
- SiFive's HiFive Unleashed
- StarFive's VisionFive 1 & 2
- Kendryte K230
- Banana Pi F3
- Milk-V Jupiter
- Milk-V Pioneer Box 128G-1T
- And more...

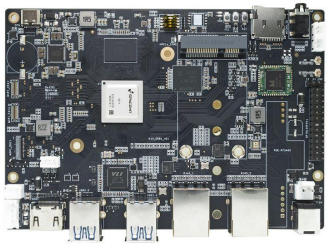












RISC-V Emulated Hardware

- QEMU User mode (for single executables)
- Full QEMU Linux system emulation
- Strategically geo-located x86 instances

6. What is Cloud-V

- Tooling shared across instances
- x86 instances available for non RISC-V related compute
- **Modeling tools** also available to run & evaluate RISC-V applications on x86 instances
- Easy to integrate with the linux environment modules tool
- Raspberry Pi 4 instances
  (for comparisons)

	Software	HiFive Unleashed	VisionFive 1 & 2	QEMU User	QEMU Linux
Languages	Python	✅	✅	✅	✅
	Ruby	✅	✅	✅	✅
	Java	✅	✅	☐	✅
	C / C++	✅	✅	✅	✅
	Go	✅	✅	☐	✅
	Rust	✅	✅	✅	✅
Build Tools	Flex	✅	✅	✅	✅
	Bison	✅	✅	✅	✅
	Ninja	✅	✅	✅	✅
	Make	✅	✅	☐	✅
	Cmake	✅	✅	☐	✅
	OpenJDK	✅	✅	✅	✅
	Autoconf	✅	✅	✅	✅
Compilers & Toolchains	RISC-V GNU Toolchain	☐	☐	✅	☐
	GCC	✅	✅	✅	✅
	LLVM / Clang	☐	☐	✅	☐
Others	OpenSSL	✅	✅	✅	✅
	Gperf	☐	✅	✅	✅

Link to Full and Updated list:

https://10x-engineers.github.io/riscv-ci-partners/Tooling

Partners / Accomplishments

RISC-V Labs (risc-v international)

- We are the first RISC-V Lab partners certified by RISC-V international! For more information visit riscv.org/risc-v-lab-partner

llama.cpp

- Open source llama.cpp from Meta (Facebook) ported to RISC-V Vector

PLCT Labs

- Running CI for nodeJS, LLVM & GCC

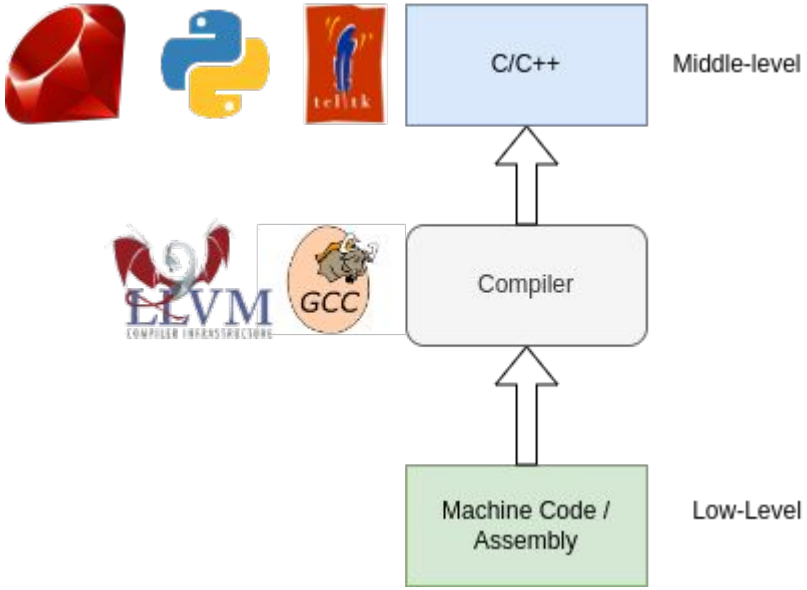
SIMDe Project

- Porting SIMDe to RISC-V Vector Extension

7. How can you start

- Reverse the execution order of applications
- High-level language interpreters are written in Middle-level language
- Gets even complex for porting bigger applications

You have to port dependencies and dependencies of dependencies



Questions

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