Open-source tools for functional testing Commercialization and Indigenous Development of Processor-Based Chips

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Professor Namal University

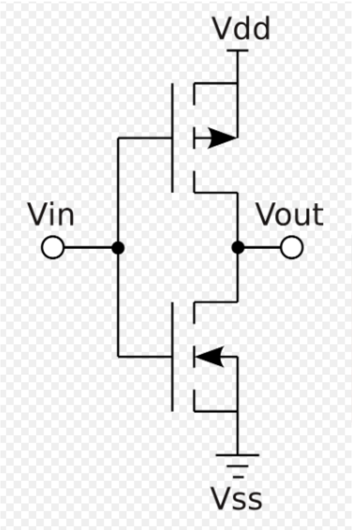
Outline

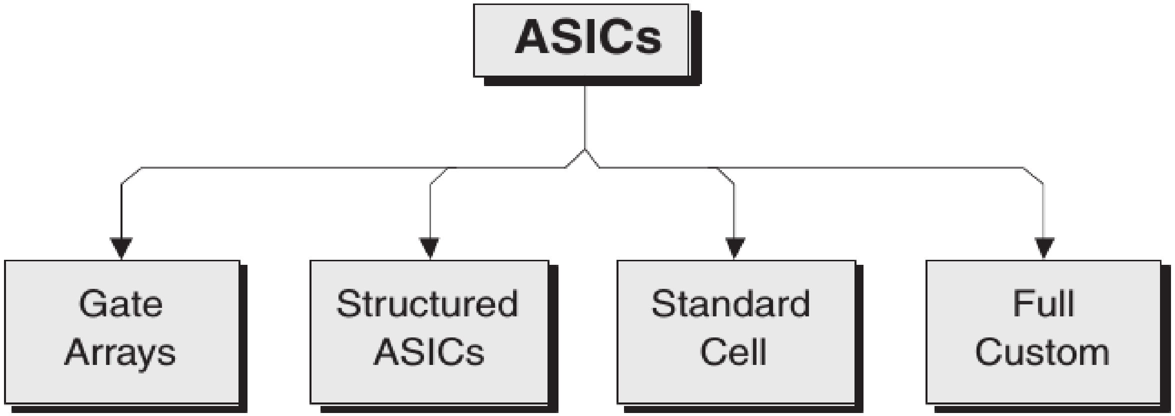
- **ASIC and FPGA**
- Open Source Process Development Kit (PDK)
- Open Source Tools for Chip Development

ASIC

ASIC: An application-specific integrated circuit (ASIC) is an integrated circuit designed for a particular use, rather than intended for general-purpose use. Processors, RAM, ROM, etc are examples of ASICs.

Fine-, medium-, and coarse-grained architectures





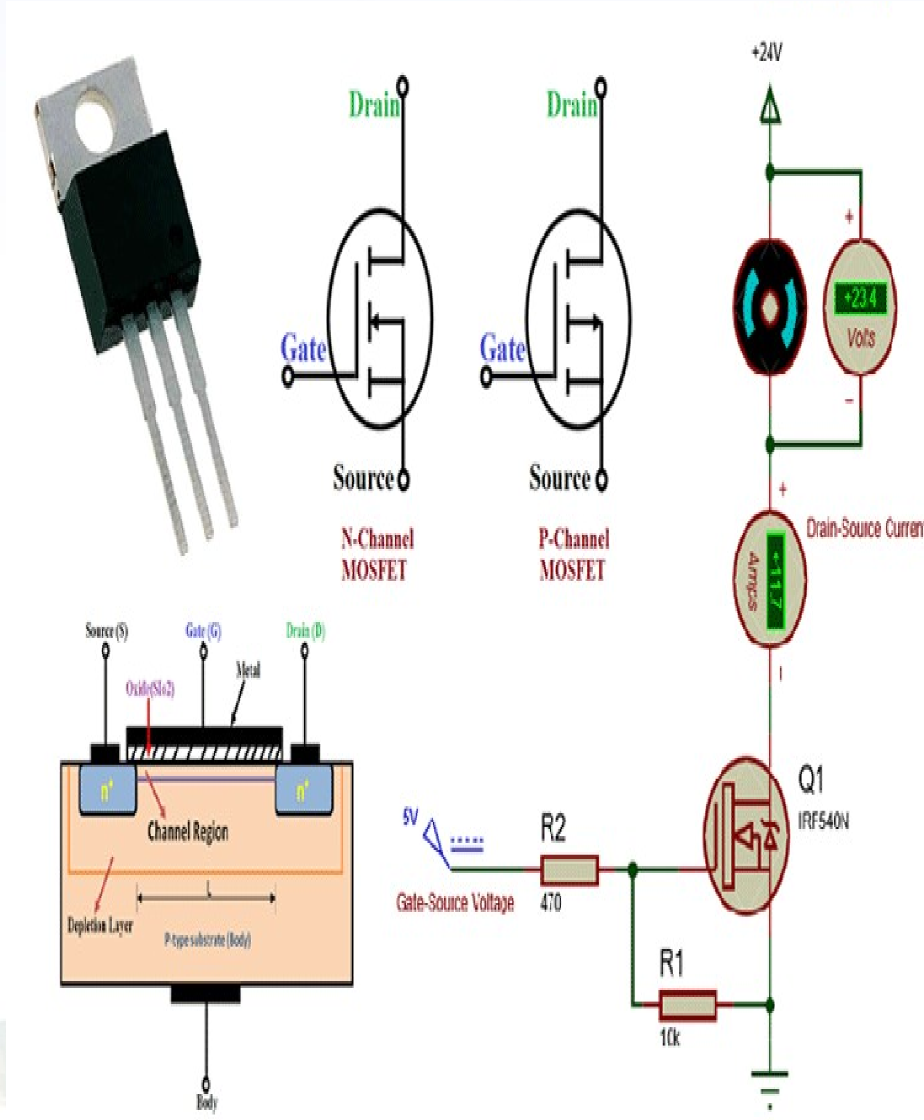
Switch: MOSFET

A MOSFET is a type of transistor is used as a switch.

Metal Oxide Silicon Field Effect Transistor.

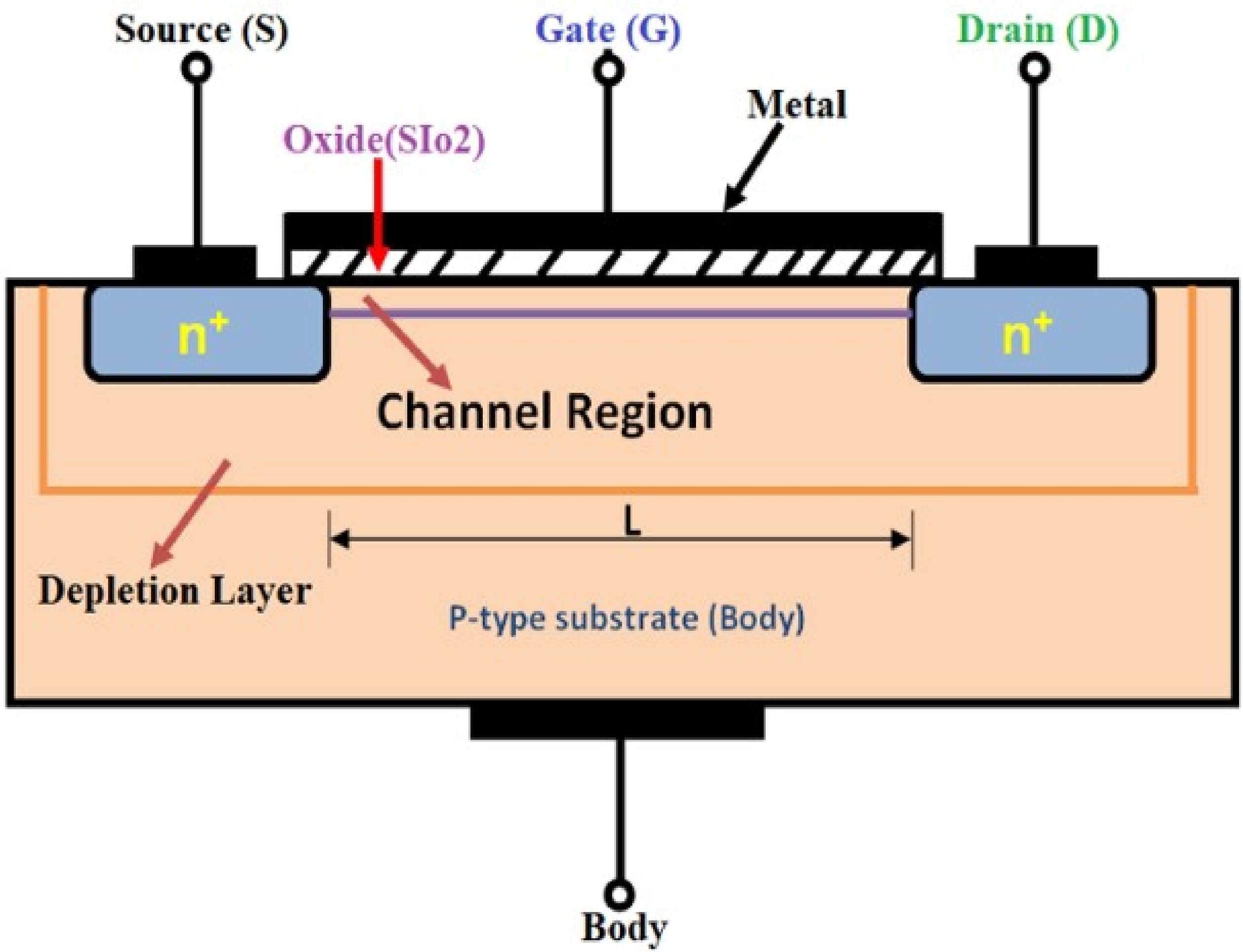
Why MOSFETS?

- ❑ Easy to manufacture in volume.
- ❑ Easy to change its size.
- ❑ It is the basic building block of modern
- ❑ Electronics.



https://components101.com/articles/mosfet-symbol-working-operation-types-and-applications

P-Type Substrate



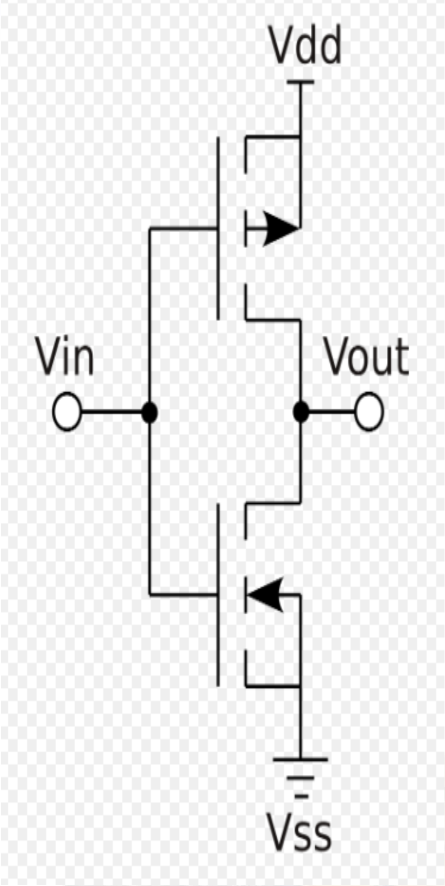
https://www.zerotoasiccourse.com/terminology/mosfet/

CMOS

CMOS Complementary metal-oxide—semiconductor (CMOS) is a type of metal-oxide—semiconductor field-effect transistor (MOSFET)fabrication process that uses complementary and symmetrical pairs of P-type and n-type MOSFETs for logic functions.

https://en.wikipedia.org/wiki/CMOS

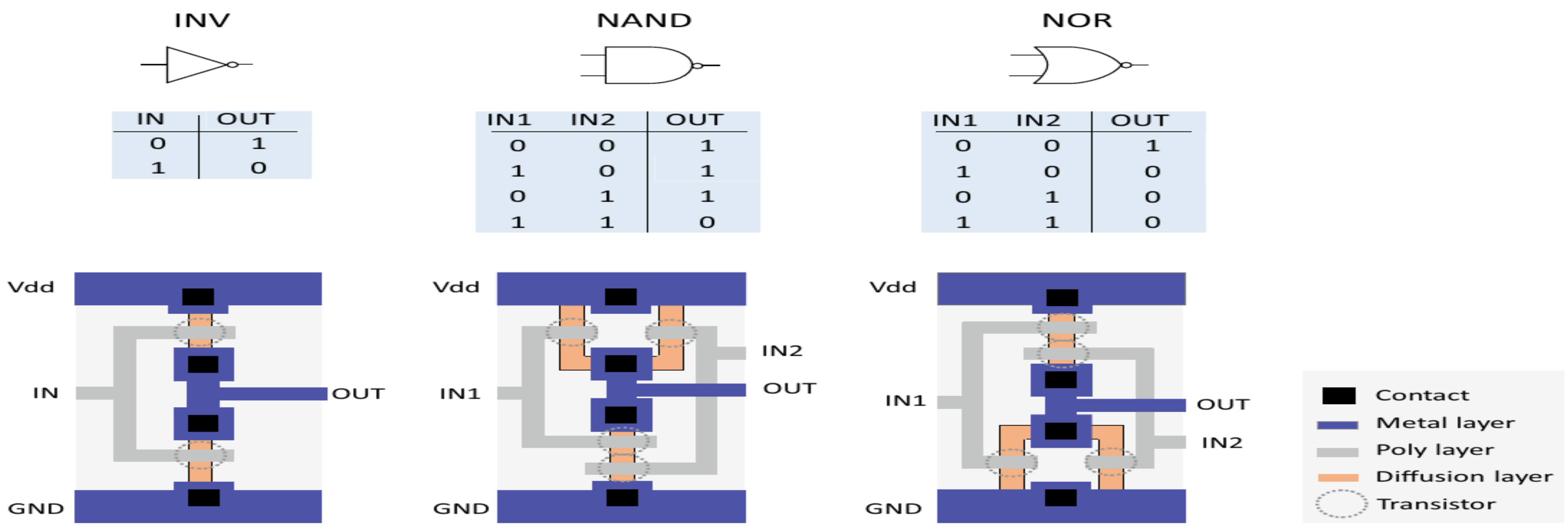
Low power compared to NMOS.



https://components101.com/articles/mosfet-symbol-working-operation-types-and-applications

Standard-cell ASIC

Standard cell ASICs are designed using predefined, reusable logic cells (standard cells) and programmable interconnections. They offer a balance between design flexibility and performance, making them suitable for a wide range of applications, including both consumer and high-performance systems.



IN	OUT
0	1
1	0

IN1	IN2	OUT
0	0	1
1	0	1
0	1	1
1	1	0

IN1	IN2	OUT
0	0	1
1	0	0
0	1	0
1	1	0

ASIC

Full Custom

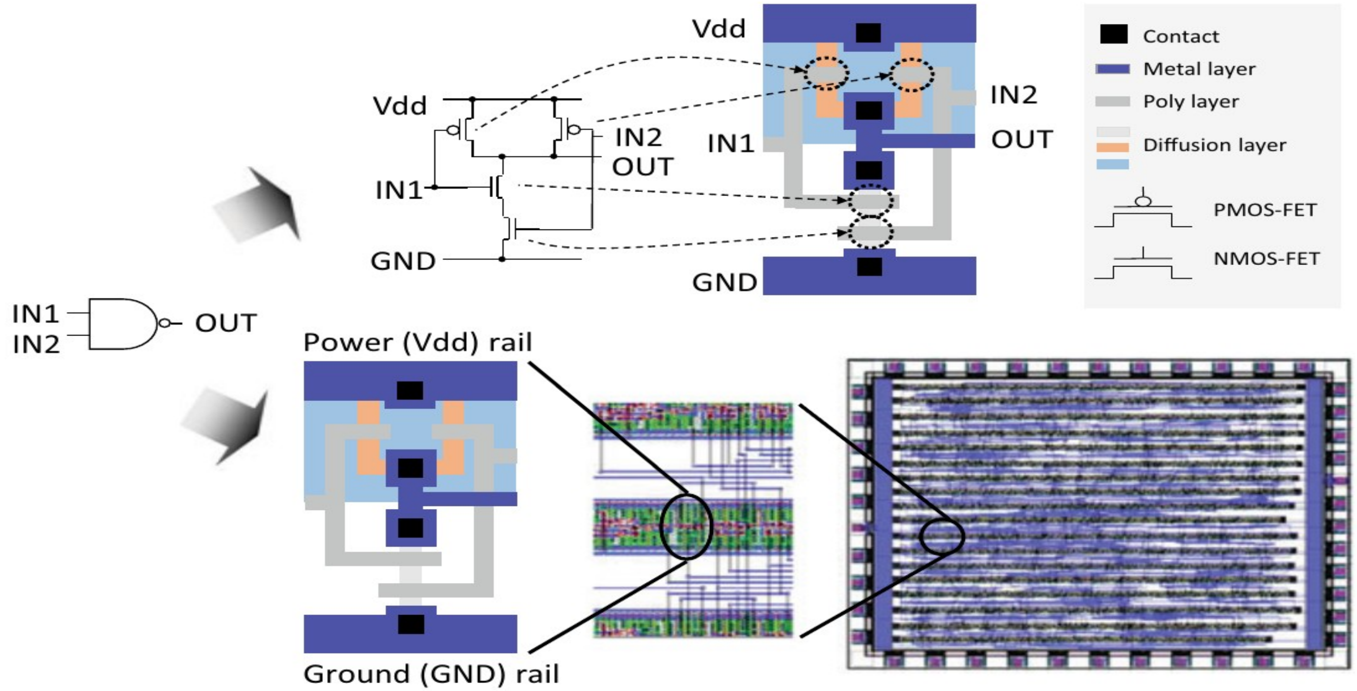
Its a design methodology in which the layout of each individual transistor on the integrated circuit (IC), and the interconnections between them, are specified.

Provides high performance, utilizes minimum area, and less power therefore its is extremely labor-intensive to implement.

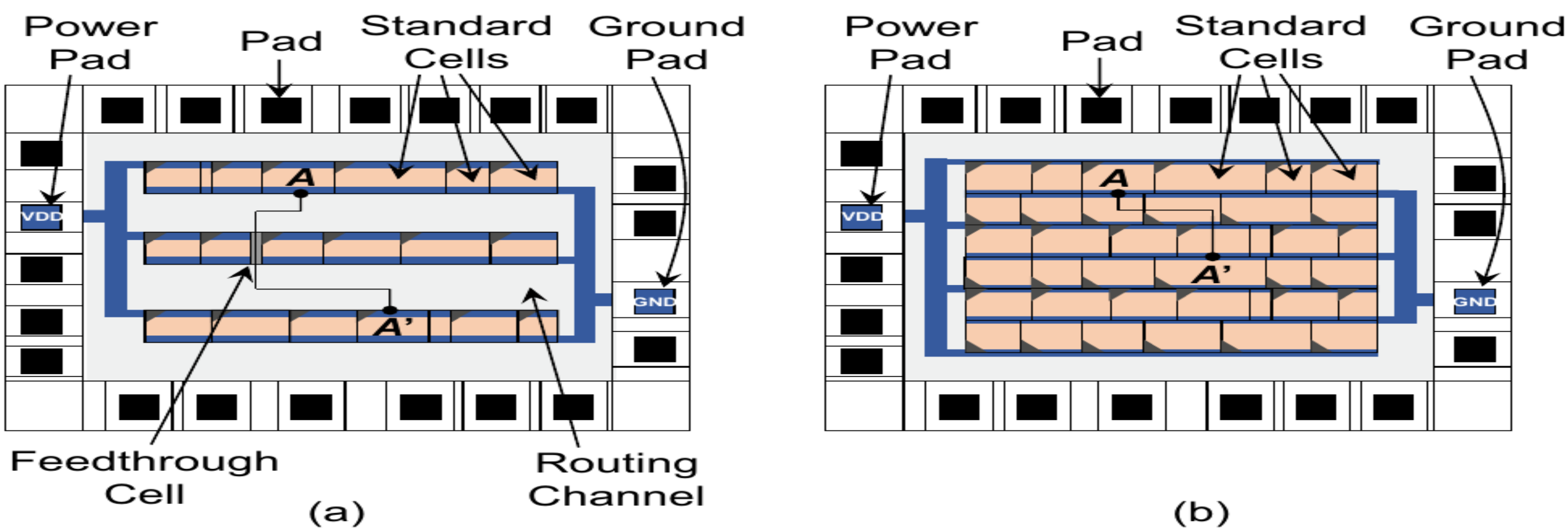
Fabricated in extremely high volumes, eg. microprocessors and a small number of application-specific integrated circuits (ASICs).

Structured

Structured ASICs offer a middle-ground between FPGAs and ASICs. **It provides predefined, fixed structures for logic, memory, and other elements, while allowing some limited customization through metal layers, interconnects, and other options. They** are partially customizable and provide a predefined, structured architecture that allows for faster time-to-market compared to full-custom ASICs while offering better performance and lower power consumption compared to FPGAs.



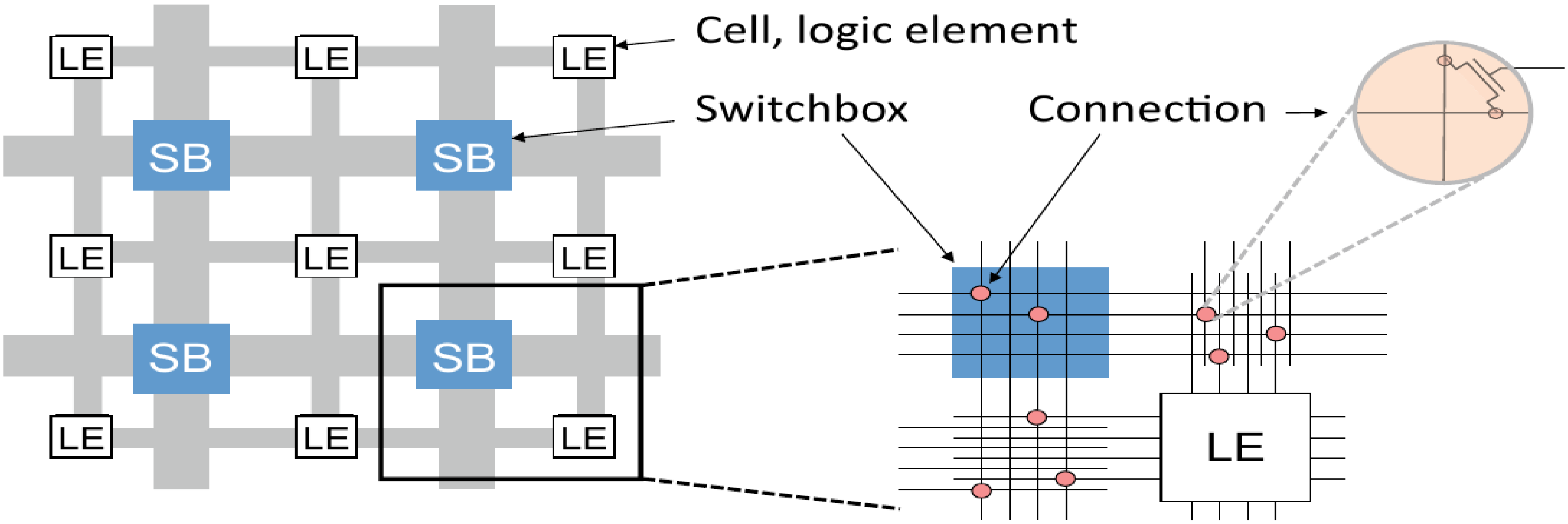
Vdd
IN2
OUT
IN1
GND
Contact
Metal layer
Poly layer
Diffusion layer
PMOS-FET
NMOS-FET
IN1
IN2
OUT
Power (Vdd) rail
Ground (GND) rail



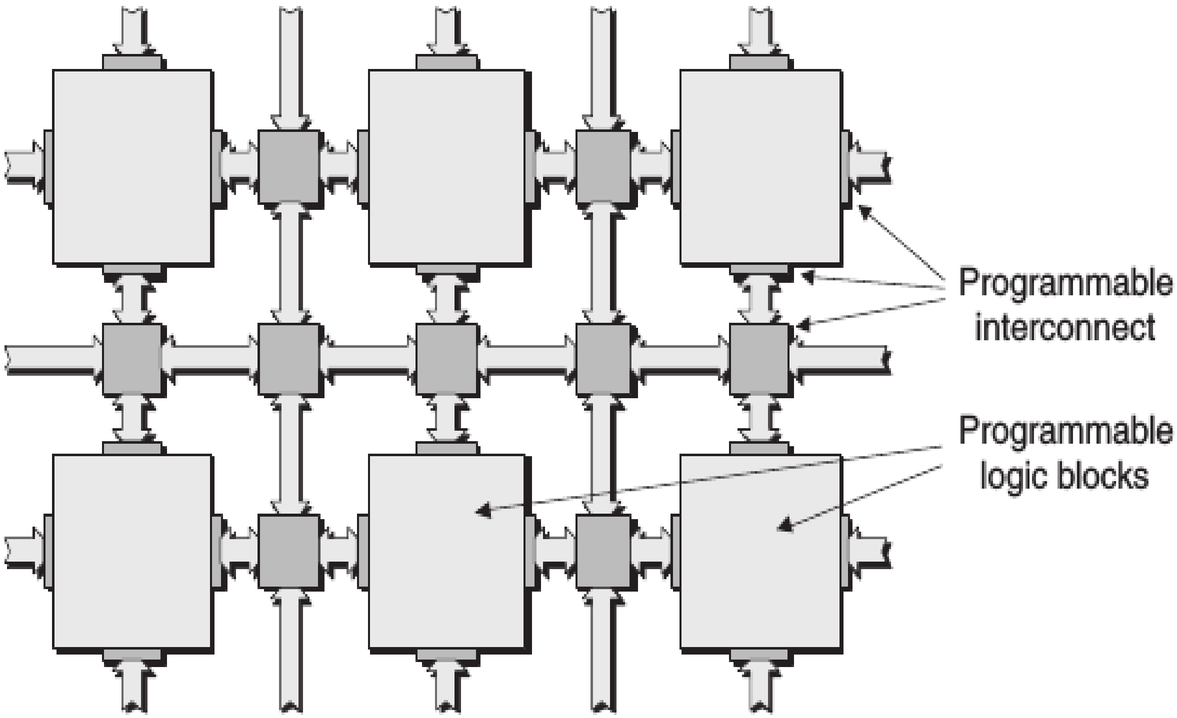
Power Pad
Pad
Standard Cells
Ground Pad
VDD
GND
A
A'
Feedthrough Cell
Routing Channel
(a)
(b)

FPGA

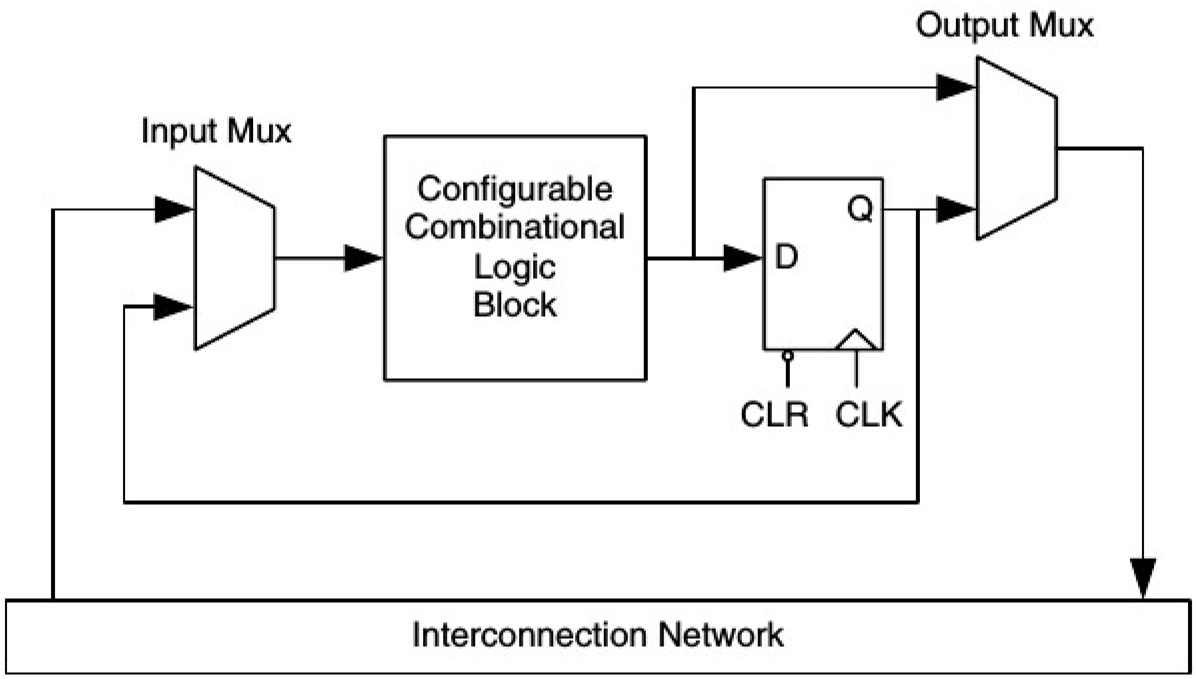
FPGA: A Field-Programmable Gate Array (FPGA) is a semiconductor device containing programmable logic components called "logic blocks", and programmable interconnects. Logic blocks can be programmed to perform the function of basic logic gates such as AND, and XOR, or more complex combinational functions such as decoders or mathematical functions.



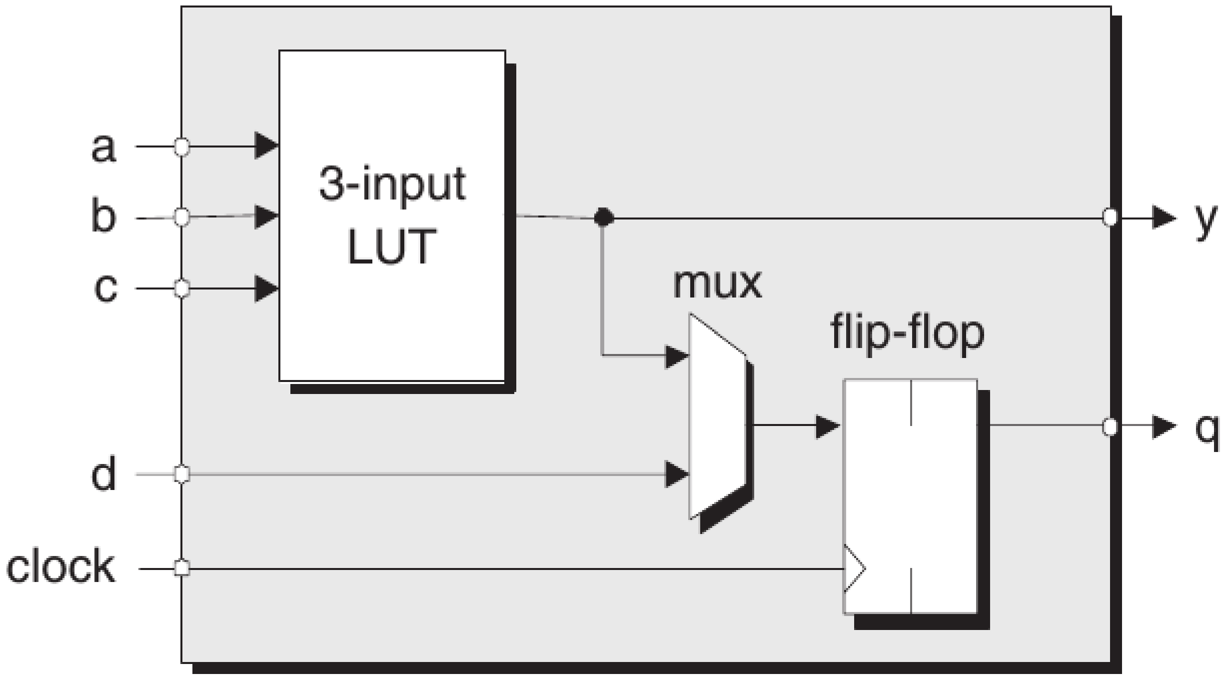
Fine-, Medium-, and Coarse-Grained Architectures



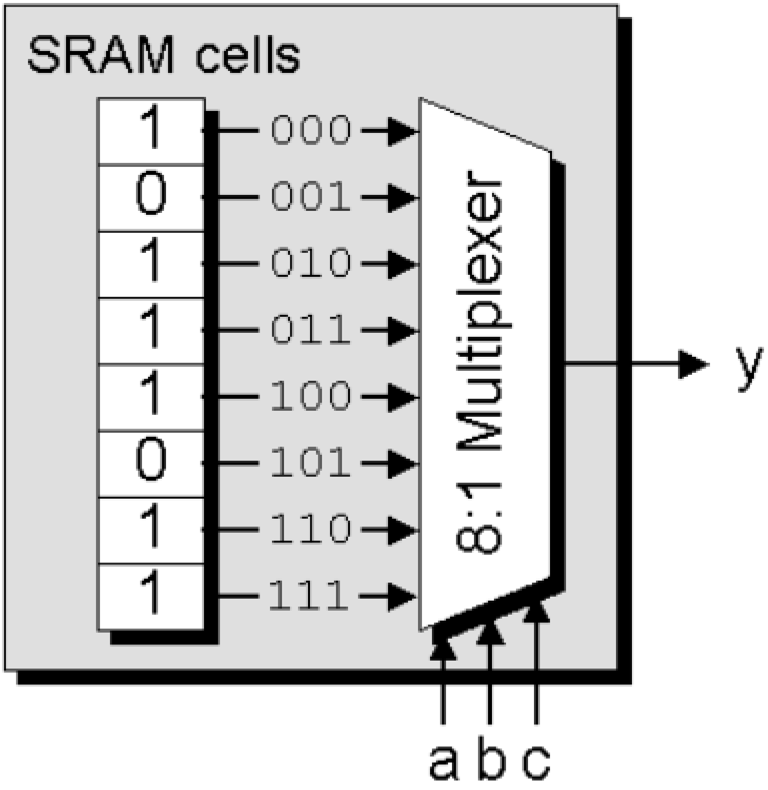
FPGA Internal Diagram



Basic Logic Slice

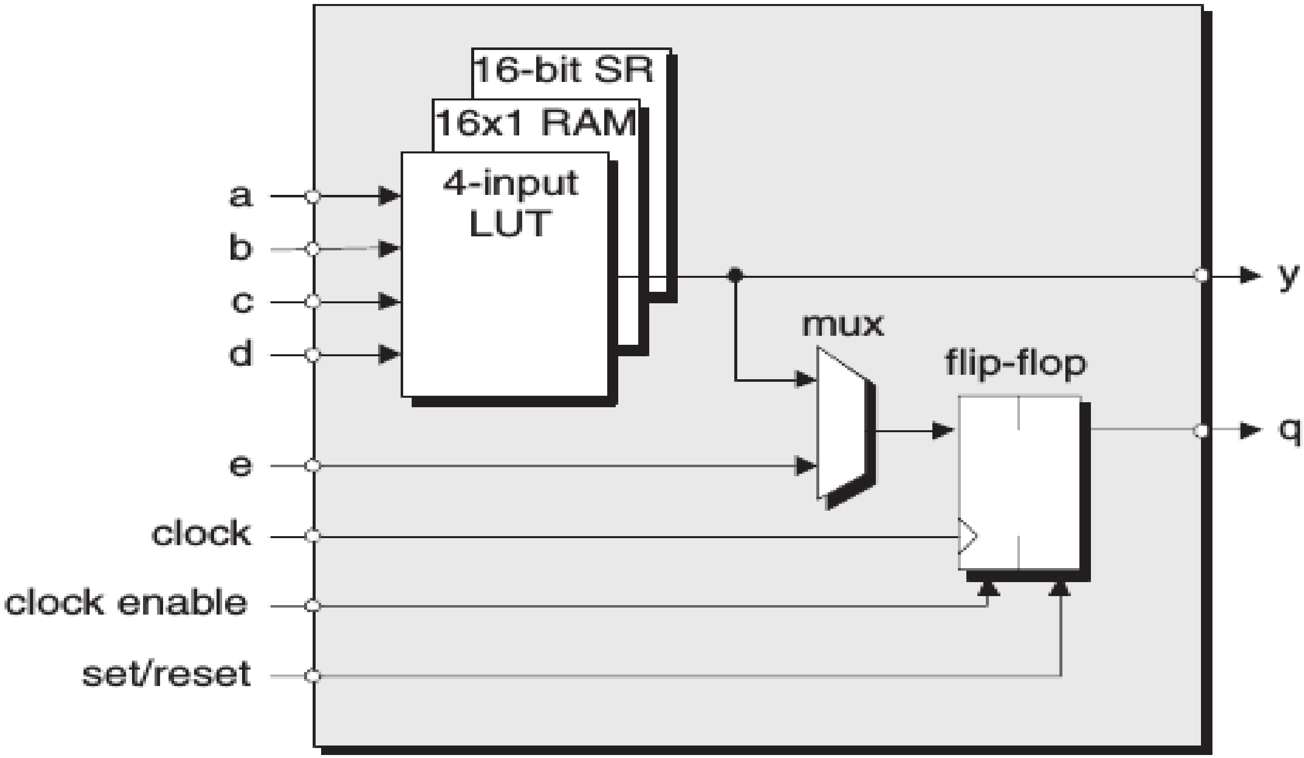


SRAM based LUT



a	b	c	y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Xilinx Logic Cell



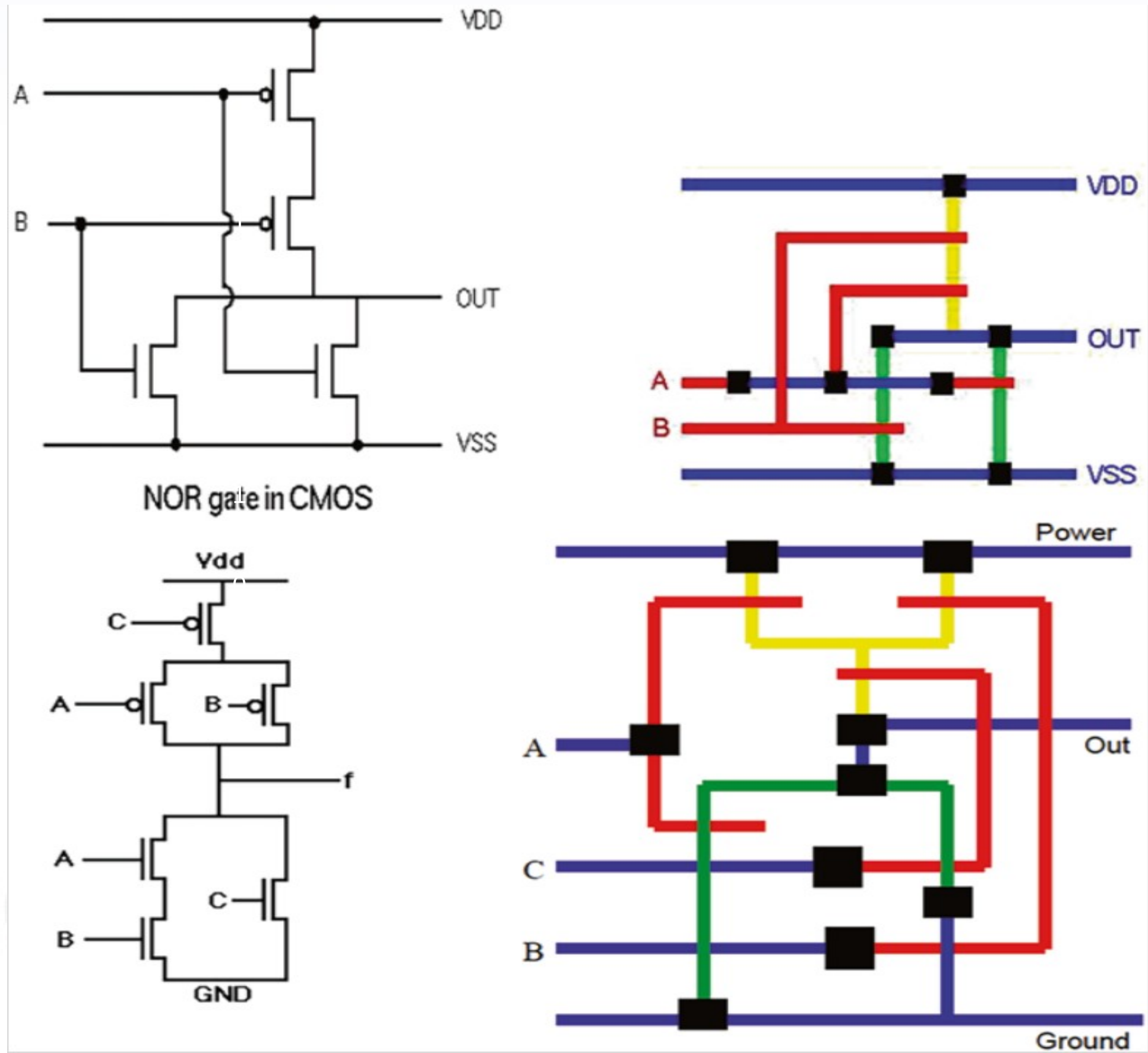
3 Input NOR Gate

A	B	C	Out
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

```
module nor3_gate (
  input A,
  input B,
  input C,
  output Y
);

assign Y = ~(A | B | C);

endmodule
```



A	B	C	Out
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

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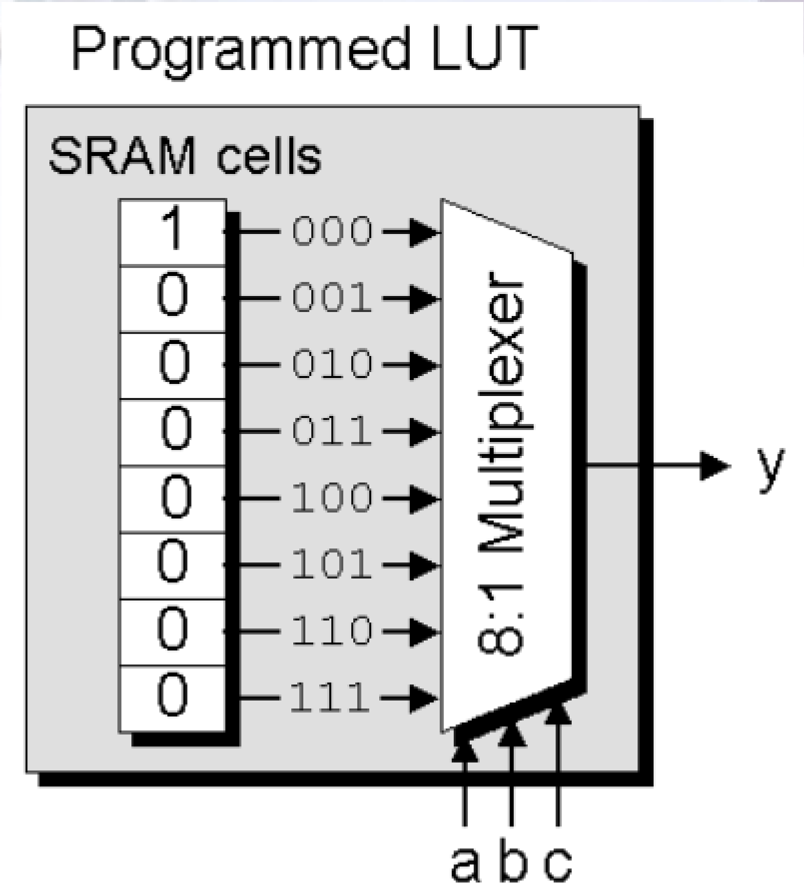
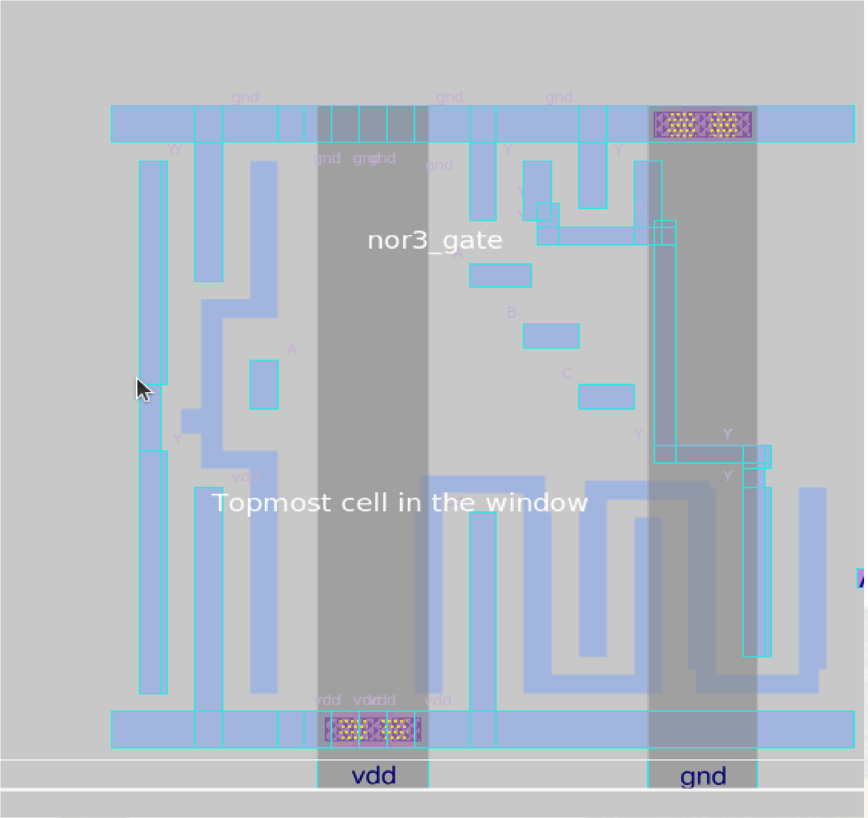


Synthesis VLSI



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- ASIC and FPGA
- **Open Source Process Development Kit (PDK)**
- Open Source Tools for Chip Development

What is in a PDK?

- **Process Design Rules**
  DRC, LVS, PEX
- **Analog Design**
  SPICE Models
  Parametric Cells
- **Behavioral Models?**
  Analog
  Digital
- **Digital Design**
  Standard Cells
  Timing models
- **Other support IP**
  Build spaces
  Basic analog
  IO Libraries
- **Extracted Data**
  SPICE/RC/LEF

A library of all specifications of a process used to fabricate chip is called process design kit (PDK)

Process Design Kits (PDKs)

PDKs are a critical component in the development of Application-Specific Integrated Circuits (ASICs). **It provides the essential information and resources required to design and manufacture custom semiconductor devices.**

Liberty (LIB):

Standard Cells Electrical Models

Library Exchange Format (LEF):

Abstract Layout of cells and finished designs and technology information

Design Exchange Format (DEF):

Design Abstract Layout

Standard Parasitic Exchange Format (SPEF):

RC values of the design wires

Graphic Design System (GDS):

Final Layout (all details)

Used to print photo masks used in fabrication

OpenPDK Files

/opt/pdks/share/pdk/sky130B/libs.ref/sky130_osu_sc_12t_ls/gds

GDS (Graphic Design System):
Store the final detailed layout of an IC design, including all the mask layers and physical details. The files are used for photomask generation and for communicating the exact layout to the semiconductor **fabrication facility (foundry)**.

LEF (Library Exchange Format):
LEF files contain an abstract representation of cell layouts, technology information, and design rules. LEF files are used by physical design tools for floorplanning, placement, and routing of custom ICs. They provide information about standard cell libraries and manufacturing constraints.

LIB (Library):
LIB files typically contain information about standard cell libraries, including cell timing, power, and functionality models. These files are used by logic synthesis tools and other design tools to optimize and simulate IC designs.

MAG (Magic Layout Editor):
MAG files are associated with the Magic Layout Editor, which is a layout tool used for designing custom ICs. MAG files may contain IC layout information and can be used for viewing and editing layouts.

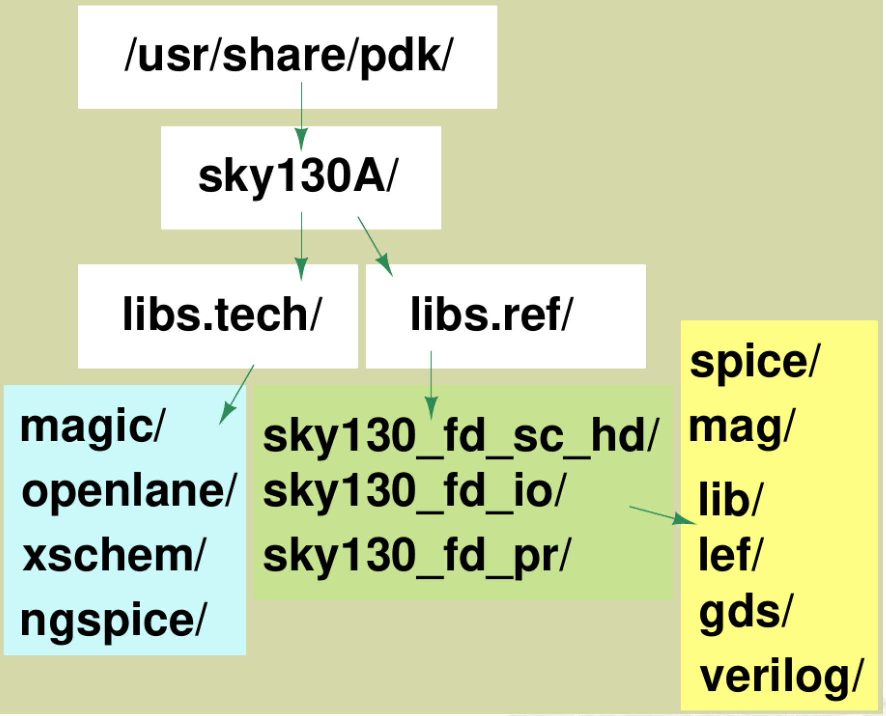
MAGLEF (Magic Layout Exchange Format):
MAGLEF for Magic Layout Editor to exchange layout information between different tools and environments. It can be used to export and import layout data.

SPICE (Simulation Program with Integrated Circuit Emphasis):
Contain circuit descriptions in the SPICE language, used for simulating the electrical behavior of ICs. Describe the components, interconnections, and electrical characteristics of the design for simulation.

TECHLEF (Technology LEF):
TECHLEF files are a specific type of LEF file that provides technology-specific information about the semiconductor process, including layer information, design rules, and materials used in the process.

Google Skywater PDK Standard Cell Library

sky130_fd_sc_hd sky130_fd_sc_hdll	High Density + Low Leakage	163 111
sky130_fd_sc_hvl	High Voltage	56
sky130_fd_sc_hs sky130_fd_sc_ms sky130_fd_sc_ls	High Speed Medium Speed Low Speed	150 150 153
sky130_fd_sc_lp	Low Power	186



FOSS 130nm Production PDK
github.com/google/skywater-pdk

Visit OpenSource PDKs

https://github.com/google/skywater-pdk

Expect a large download! ~7GB at time of 2 Years before.

SUBMODULE_VERSION=latest make submodules -j3 || make submodules -j1

make

Process Design Kit

A Process Design Kit (PDK) is a library of basic component generated by the foundry to give open access to their generic process for fabrication.

A designer can also create own building blocks, but the designer must follow the fabrication rules of the foundry to be able to use a custom component from a particular foundry.

Among others, the rules usually include:

- Material stack (types of layers and thickness)
- Minimum distance between optical components (like gaps between waveguides)
- Maximum etching depths
- Metallization and electrical probes (how to place the metal, metal layers allowed)
- Feature size (size of waveguides, holes, active areas, etc.)

PDK libraries

Basic Device Libraries:

- Transistors: Includes models for NMOS (n-channel metal-oxide-semiconductor) and PMOS (p-channel metal-oxide-semiconductor) transistors.
- Diodes: Models for various types of diodes such as Schottky diodes, pn-junction diodes, etc.
- Resistors: Models for different types of resistors with varying resistance values.
- Capacitors: Models for capacitors with different capacitance values.

Analog and Mixed-Signal Libraries:

- Op-amps: Operational amplifier models for analog circuit design.
- Comparators: Models for voltage comparators used in analog and mixed-signal circuits.
- Voltage references: Models for generating stable reference voltages.
- Phase-locked loops (PLLs): Models for PLL circuits used in clock generation and synchronization.

Digital Libraries:

- Logic Gates: Models for basic logic gates such as AND, OR, XOR, NAND, NOR, etc.
- Flip-Flops and Latches: Models for sequential logic elements used in digital circuit design.
- Multiplexers and Demultiplexers: Models for data multiplexing and demultiplexing circuits.
- Counters and Shift Registers: Models for digital counters and shift register circuits.

IO Libraries:

- Input/Output Buffers (IOBs): Models for input and output buffer circuits used for interfacing with external devices.
- Pad Cells: Models for bonding pad cells used for wire bonding or flip-chip packaging.

Memory Libraries:

- Static Random Access Memory (SRAM): Models for SRAM cells used for on-chip memory.
- Read-Only Memory (ROM): Models for ROM cells used for storing fixed data.
- Registers and Register Files: Models for register cells and register file arrays used in digital design.

Custom and Specialized Libraries:

- Custom Cells: User-defined cells tailored to specific design requirements.
- Analog Blocks: Pre-designed analog building blocks such as amplifiers, filters, oscillators, etc.
- Specialized Cells: Cells designed for specific applications such as high-speed interfaces, low-power circuits, etc.

Design your Own PDK

Define Process Parameters:

Specify the process parameters for your CMOS technology, including the minimum feature sizes, transistor dimensions, doping concentrations, oxide thicknesses, and other fabrication parameters.

Device Models:

Develop SPICE models for the CMOS devices (NMOS and PMOS transistors) based on the process parameters. These models should accurately represent the behavior of the devices under different operating conditions (DC, AC, transient).

Layout Design Rules:

Define layout design rules that specify the geometric constraints for laying out CMOS circuits. This includes rules for minimum feature sizes, spacing, metal layer stack-up, via placement, and other layout constraints.

Extraction Rules:

Define rules for extracting electrical parameters from layout designs. This includes parameters such as resistance, capacitance, parasitic capacitance, and parasitic resistance. The extraction rules should ensure accurate simulation results.

Library Components:

Create libraries of standard CMOS components such as transistors, diodes, resistors, capacitors, and interconnect structures. These libraries should include layout cells (symbols) and associated SPICE models.

Technology Files (Tech Files):

Write technology files (tech files) that encapsulate the process parameters, device models, layout design rules, and extraction rules. Tech files are typically written in a specific format supported by layout design tools like Magic.

Integration with Layout Tools:

Integrate your PDK library with layout design tools like Magic by importing the technology files and configuring the tool to use your custom PDK. This allows designers to access your PDK library when creating layouts and performing simulations.

Documentation and Support:

Provide comprehensive documentation for your PDK library, including user guides, manuals, and tutorials. Additionally, offer support to users who may have questions or encounter issues when using your PDK.

Validation and Testing:

Test your PDK library thoroughly to ensure that it meets the required specifications and functionality. This includes verifying device models, layout design rules, extraction accuracy, and compatibility with layout design tools.

90NM PDK

Minimum Feature Size (MFS): Approximately 90 nanometers (nm). This is the smallest feature size that can be reliably manufactured in the process.

Gate Oxide Thickness: Around 1.2 nanometers (nm). This is the thickness of the gate oxide layer in MOSFETs.

Channel Length (L): Typically around 45nm for both NMOS and PMOS transistors. This is the length of the channel region in MOSFETs.

Doping Concentrations: Varies depending on the specific design requirements, but typically in the range of 1e17 to 1e20 atoms/cm^3 for both NMOS and PMOS transistors.

Threshold Voltage (Vt): Typically around 0.3 to 0.5 volts (V) for both NMOS and PMOS transistors.

Supply Voltage (Vdd): Usually around 1.0 to 1.2 volts (V) for digital CMOS circuits.

Metal Layers: Multiple metal layers (e.g., M1, M2, M3) for interconnect routing, with typical metal pitch of around 180nm.

Dielectric Constant (k): The dielectric constant of the interlayer dielectric material, which affects capacitance between metal layers.

Interconnect Resistance and Capacitance: Depends on the metal layer thickness, width, and spacing.

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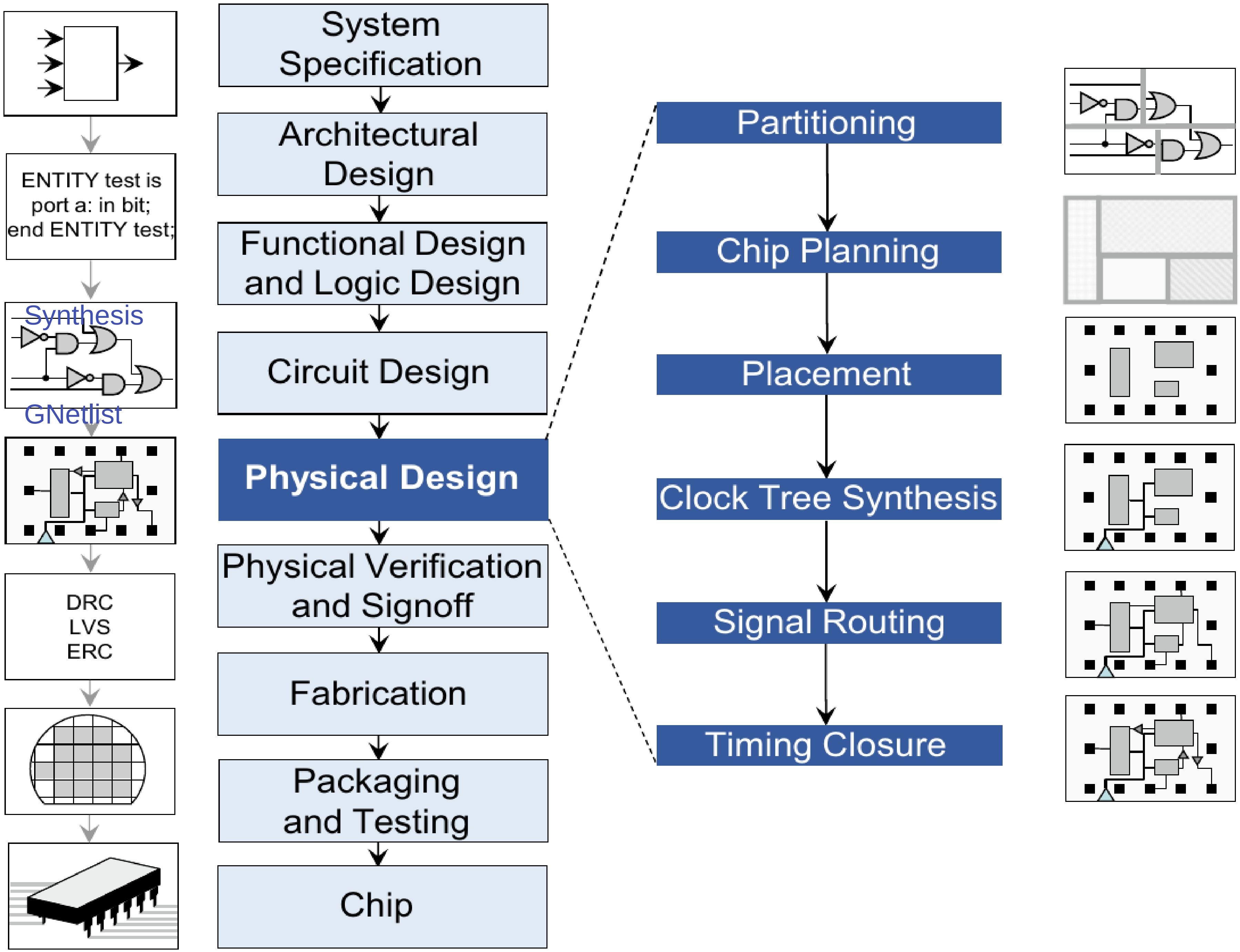
System Specification
Architectural Design
Functional Design and Logic Design
Circuit Design
Physical Design
Physical Verification and Signoff
Fabrication
Packaging and Testing
Chip
ENTITY test is
port a: in bit;
end ENTITY test;
Synthesis
GNetlist
DRC
LVS
ERC
Partitioning
Chip Planning
Placement
Clock Tree Synthesis
Signal Routing
Timing Closure

Physical Design

- **Partitioning** breaks up a circuit into smaller subcircuits or modules, which can each be designed or analyzed individually.
- **Floorplanning** determines the shapes and arrangement of subcircuits or modules, as well as the locations of external ports and IP or macro blocks.
- **Power and ground routing** often intrinsic to floorplanning, distributes power (VDD) and ground (GND) nets throughout the chip.
- **Placement** finds the spatial locations of all cells within each block.
- **Clock network synthesis** determines the buffering, gating (e.g., for power management), and routing of the clock signal to meet prescribed skew and delay requirements.
- **Global Routing** allocates routing resources that are used for connections; example resources include routing tracks in global cells (gcells).
- **Detailed Routing** assigns routes to specific metal layers and routing tracks within the global routing resources.
- **Timing Closure Optimizes** circuit performance by specialized placement and routing techniques.

Physical Verification and PDKs

After physical design is completed, the layout is verified to ensure correct electrical and logical functionality.

–**Design rule checking (DRC)** verifies that the layout meets all technology-imposed constraints. DRC also verifies layer density for uniform chemical-mechanical polishing (CMP). **PDKs contain comprehensive data about the semiconductor process technology used in the foundry.**

– **Layout vs. schematic (LVS)** checking verifies the functionality of the design. To do this, the layout is used to derive (i.e., reverse engineer) a netlist, which is compared with the original netlist produced from logic synthesis or circuit design. **PDKs include information about the geometric representations of standard cells and layout elements.**

– **Parasitic extraction** derives electrical parameters of the layout elements from their geometric representations; the resulting accurate analog netlist is used to verify the electrical characteristics of the circuit. **PDKs provide data on the physical properties of the semiconductor process, including details on layers, materials, and device geometries.**

– **Antenna rule checking** seeks to prevent antenna effects, which may damage transistor gates during manufacturing plasma-etch steps through the accumulation of excess charge on metal wires that are not connected to PN junction nodes. **PDK provides rules and guidelines for preventing antenna effects, which occur due to the accumulation of charge on unconnected metal wires during plasma-etch manufacturing steps.**

– **Electrical Rule checking (ERC)** verifies the correctness of power and ground connections, and that signal transition times (slew), capacitive loads, and fanouts are appropriately bounded. **PDKs provide information about standard cell libraries, including power and ground connections, signal transition times (slew rates), capacitive loads, and fanout limits.**

Fabrication

The final DRC-/LVS-/ERC-clean layout, usually represented in the GDSII or OASIS Stream format, is sent for manufacturing at a dedicated silicon foundry (fab). The handoff of the design to the manufacturing process is called tapeout, even though data transmission from the design team to the silicon fab no longer relies on magnetic tape [5]. Generation of the data for manufacturing is sometimes referred to as streaming out, reflecting the use of the GDSII or OASIS Stream format.

Lab: View Klayout (GDS)

ASIC Vs FPGA

Speed

Cost

Size/Area

Time to Market

Power

Programming

Testing Verification

Packaging and Testing

After dicing, functional chips are typically packaged. Packaging is configured early in the design process, and reflects the application along with cost and form factor requirements. Package types include dual in-line packages (DIPs), thin small-outline packages (TSOPs), and ball grid arrays (BGAs).

After a die is positioned in the package cavity, its pins are connected to the package’s pins, e.g., with wire bonding or solder bumps (flip-chip). The package is then sealed.

RISCV System VLSI Problems

- RISC-V enables hardware innovation by smaller organizations
  - No architecture licensing fee, no limits on customizing ISA
  - Open source software ecosystem with compilers, OS…
- But creating commercially competitive accelerator is challenging
  - Leading edge semiconductor design is extremely expensive
  - Novel ideas take time to gain momentum and volume in market

Fabrication Processes

Economic Consideration

- Cost of Silicon Device
    - Recurring Cost
    - Non-recurring Cost

5nm Chip NRE 500M$

- 50M devices => 10$/device
- 100K => $5000/device

Solution of Cost and Performance

- Multiple Chips on Substrate Multi-Project Wafer (MPW) (Open Chiplet Initiative)
- Chip/wafer Stacking (TSMC 3D Fabric) to increase performance

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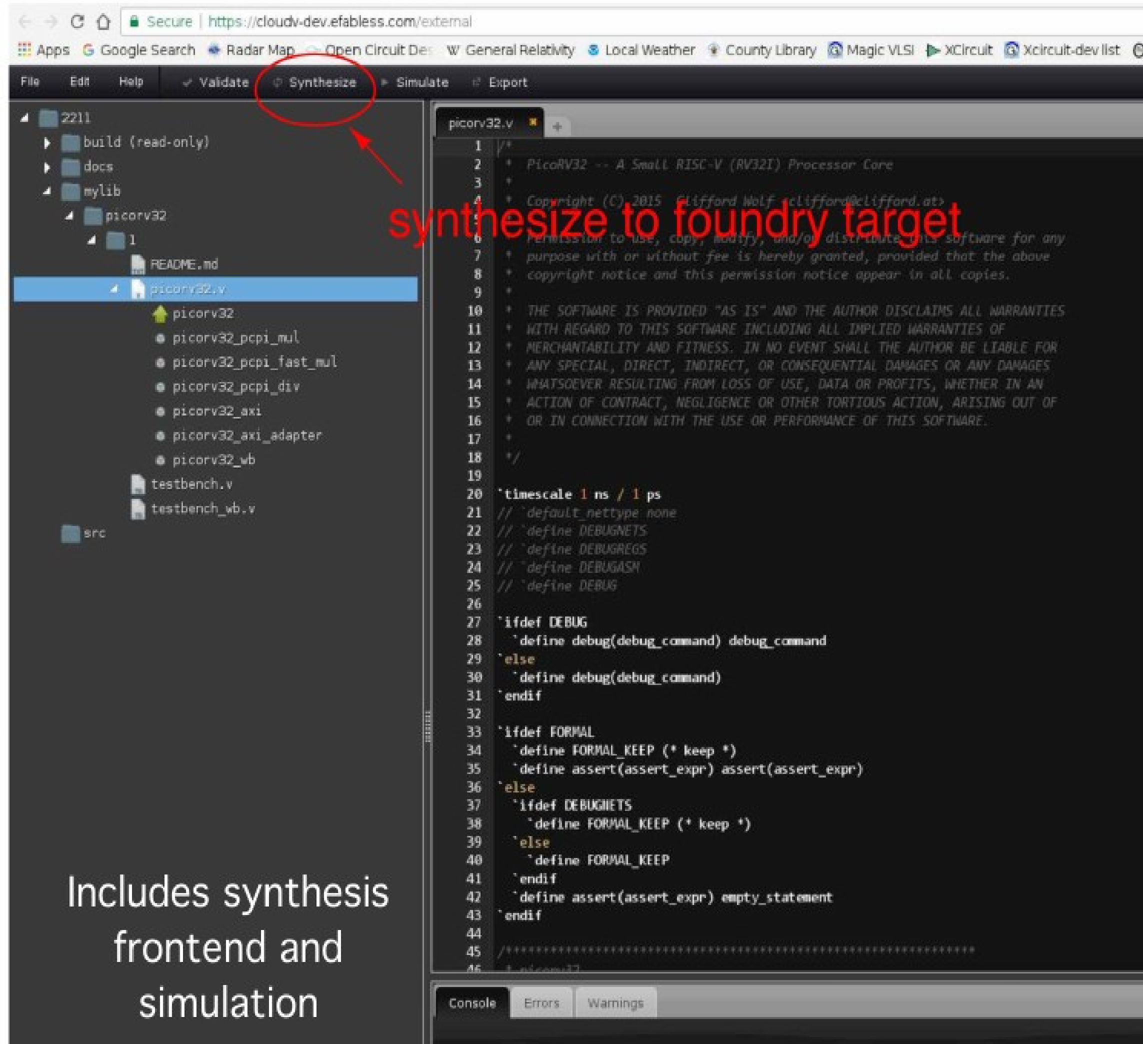
efabless

efabless' CloudV-based Design Environment

1. "Soft IP" from the catalog can be viewed in cloudV.

2. The cloudV tool can simulate verilog source and testbenches, and synthesize to a foundry process target digital library.

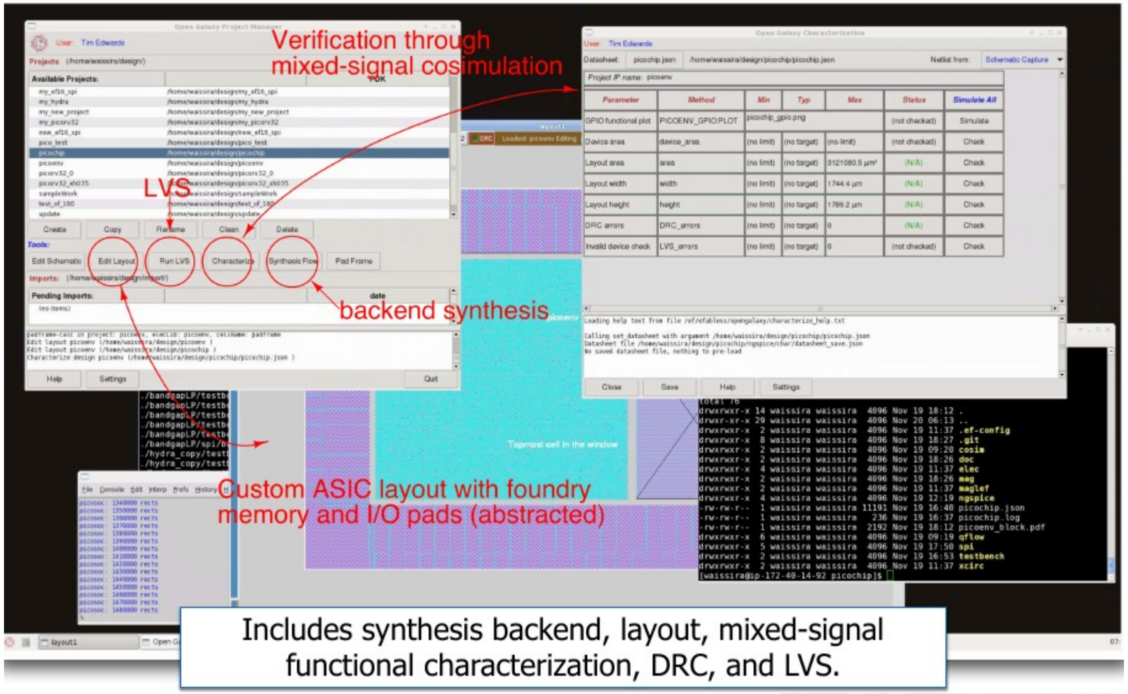
3. Synthesized netlists can be exported to the efabless Open Galaxy platform.



Source: Efabless 7th RISC-V Workshop

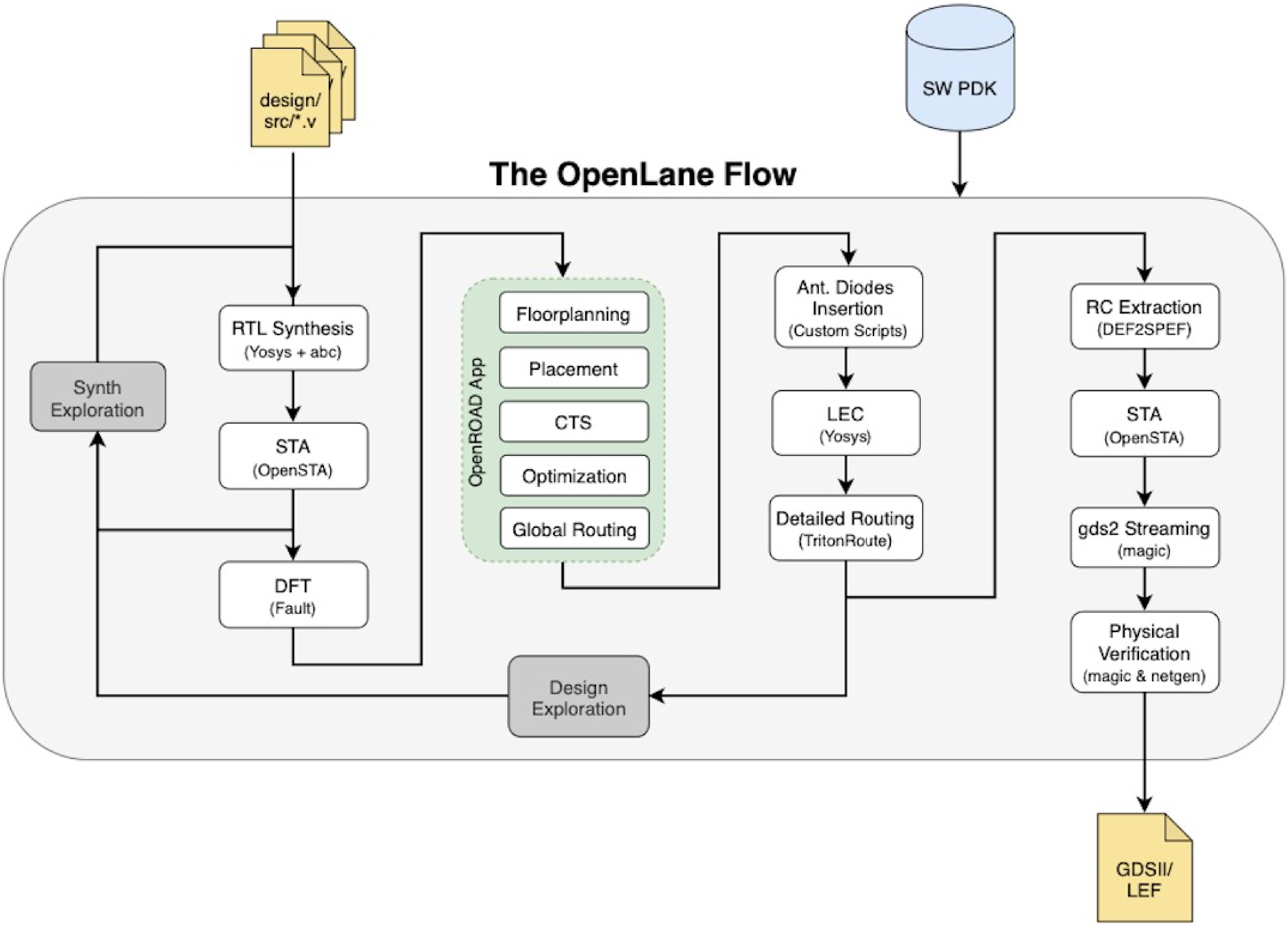
efabless’ Open Galaxy Design Environment

1. Hard IP" from the IP catalog can be viewed in Open Galaxy as an imported project or can be used in a new or existing project.
2. Verification through mixed-signal cosimulation
3. Synthesized netlists from cloudV can be imported as a project and taken through backend synthesis to a completed layout.
4. backend synthesis
5. Designs can be verified through DRC, LVS, STA, and mixed-mode simulation.
6. Custom ASIC layout with foundry memory and I/O pads



FOS VLSI Design Suits

Tool	Supported Design Approach	Supported Languages	Features	Supported Nanometer Technology	Output Support for ASIC Foundry	Supported Foundar
Qflow	RTL, Gate-Level	Verilog, VHDL	Complete ASIC design flow	180nm, 130nm, 90nm, 65nm	GDS, LEF, DEF, Verilog, VHDL	Various, including MPW services
OpenROAD	RTL, Gate-Level	Verilog	Open-source digital ASIC design flow	180nm, 130nm, 90nm, 65nm	GDS, LEF, DEF, Verilog, VHDL	SkyWater Technology Foundry, etc.
OpenLANE	RTL, Gate-Level	Verilog	Open-source Digital ASIC flow including P&R	180nm, 130nm, 90nm, 65nm	GDS, LEF, DEF, Verilog, VHDL	SkyWater Technology Foundry, etc.



design/
src/*.v
SW PDK
The OpenLane Flow
RTL Synthesis
(Yosys + abc)
STA
(OpenSTA)
DFT
(Fault)
Synth
Exploration
OpenROAD App
Floorplanning
Placement
CTS
Optimization
Global Routing
Ant. Diodes
Insertion
(Custom Scripts)
LEC
(Yosys)
Detailed Routing
(TritonRoute)
Design
Exploration
RC Extraction
(DEF2SPEF)
STA
(OpenSTA)
gds2 Streaming
(magic)
Physical
Verification
(magic & netgen)
GDSII/
LEF

Qflow ASIC Design Tool