BSC~Microsoft Research Centre

Introduction to Parallel Computer Architecture

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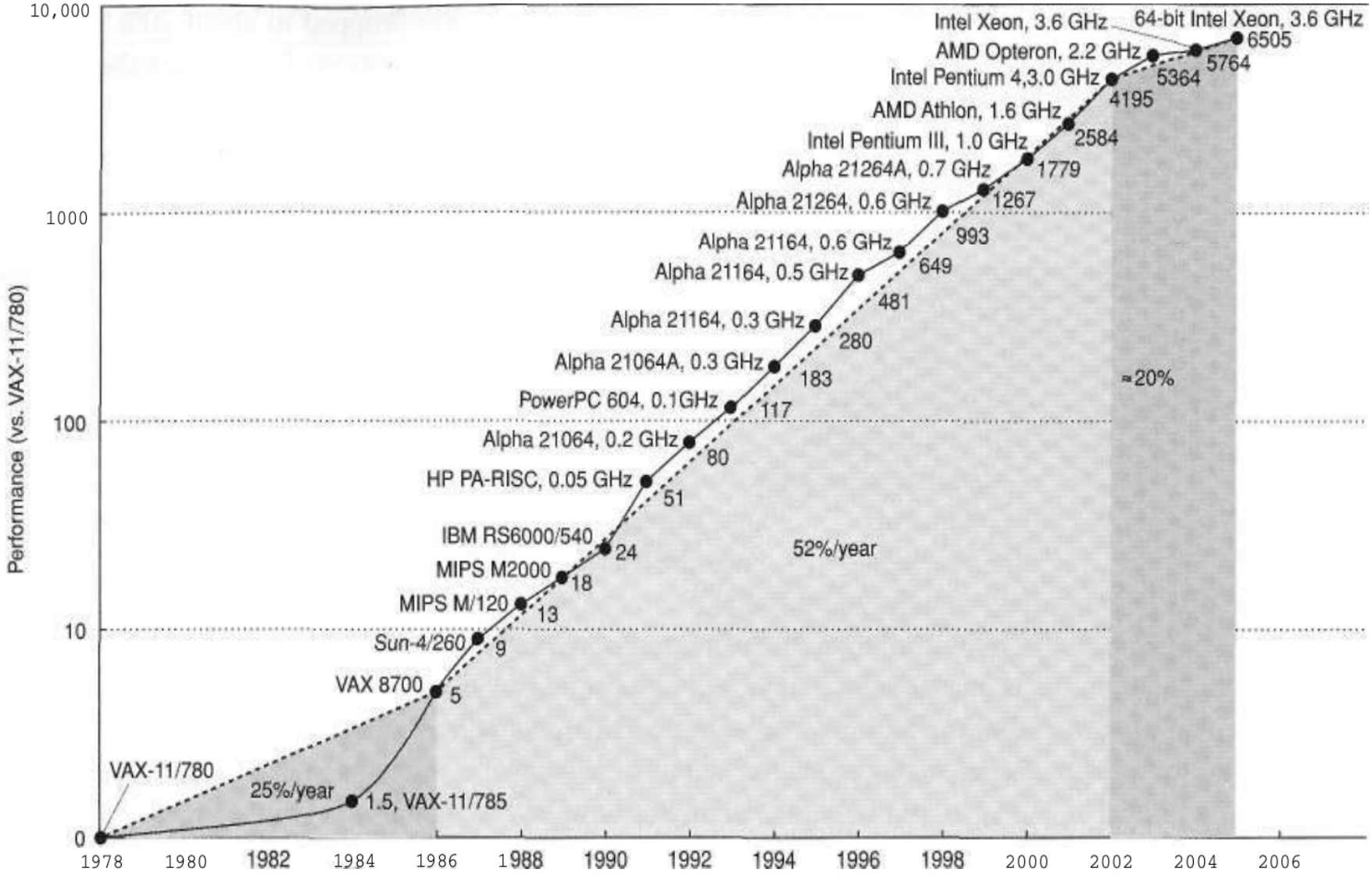

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Price

Feature	Desktop	Server	Embedded
Price of system	$500-$5000	$5000-S5,000,000	$10-$100,000 (including network routers at the high end)
Price of microprocessor module	$50-$500 (per processor)	$200-$ 10,000 (per processor)	$0.01-$100 (per processor)
Critical system design issues	Price-performance, graphics performance	Throughput, availability, scalability	Price, power consumption, application-specific performance

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Types of Computers

- Desktop Computer
- Servers
- Embedded Computer

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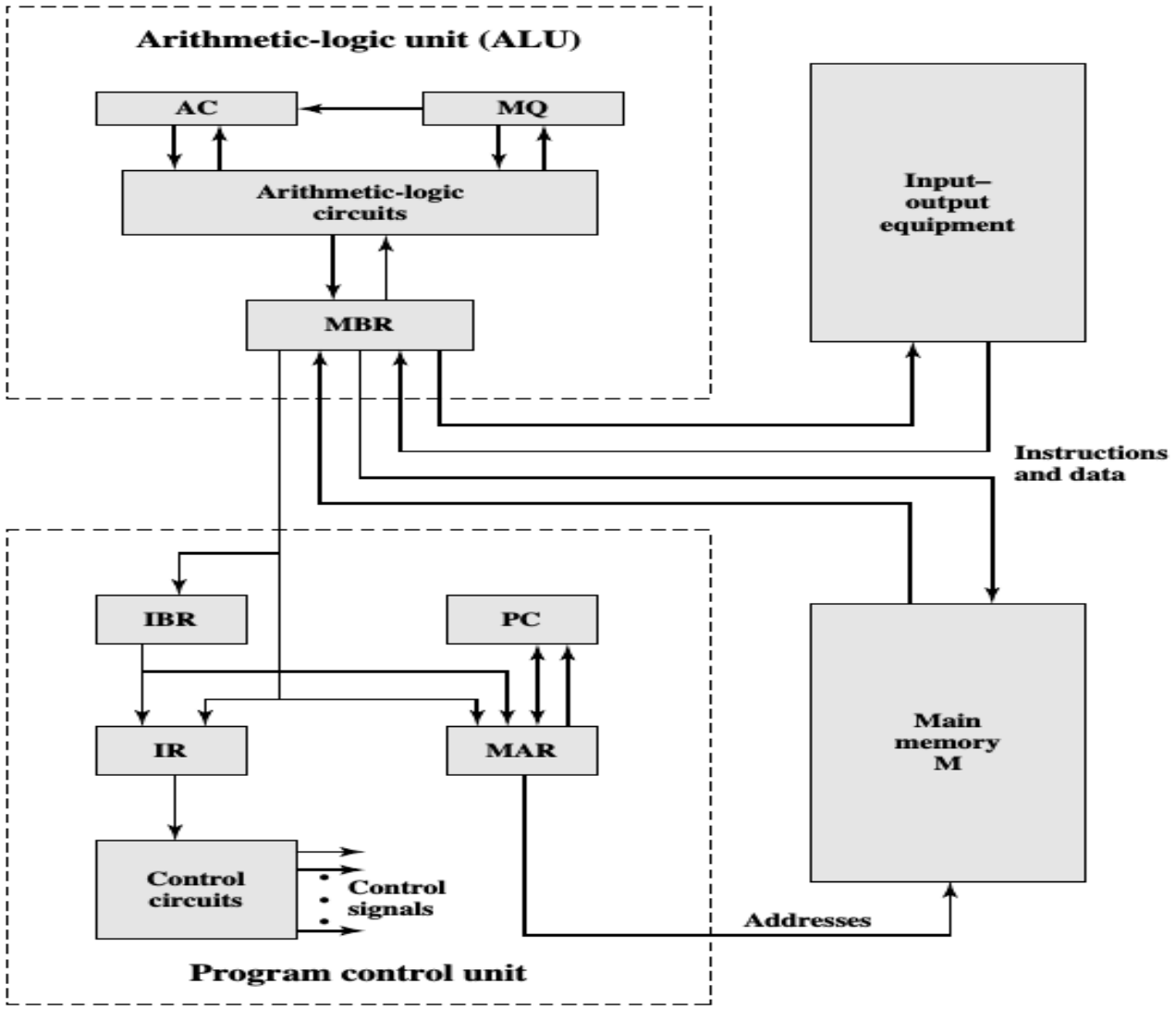
Basic Computer Architecture



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Basic Computer Register

- **Memory buffer register (MBR)**: Contains a word to be stored in memory or sent to the I/O unit, or is used to receive a word from memory or from the I/O unit.
- **Memory address register (MAR)**: Specifies the address in memory of the word to be written from or read into the MBR.
- **Instruction register (IR)**: Contains the 8-bit opcode instruction being executed.
- **Instruction buffer register (IBR)**: Employed to hold temporarily the right-hand instruction from a word in memory.
- **Program counter (PC):** Contains the address of the next instruction-pair to be fetched from memory.
- **Accumulator (AC): and multiplier quotient (MQ)**: Employed to hold temporarily operands and results of ALU operations. For example, the result of multiplying two 40-bit numbers is an 80-bit number; the most significant 40 bits are stored in the AC and the least significant in the MQ.

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Defining Computer Architecture

- In the past, the term computer architecture often referred only to instruction set design.
- Now System Architecture is much more than instruction set design, and the technical hurdles in the other aspects.

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Instruction Set Architecture

- Class of ISA – GPP Register
- Memory Addressing – Byte Adress
- Addressing Mode
- Type and Size of Operands
- Operation
- Control Flow Instruction

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Instruction Set Architecture

- Class of ISA – GPP Register
- Memory Addressing – Byte Address
  - **Load Store, Scatter Gather s**
- Addressing Mode
- Type and Size of Operands
- Operation
- Control Flow Instruction

Benchmarks

- Benchmarks are used to measure performance of real applications.
- **Kernels**, which are small, key pieces of real application.
- **Toy programs,** which are 100-line programs from beginning programming assignments, such as quicksort;
- **Synthetic benchmarks,** are fake programs invented to try to match the profile and behavior of real applications, such as Dhrystone.

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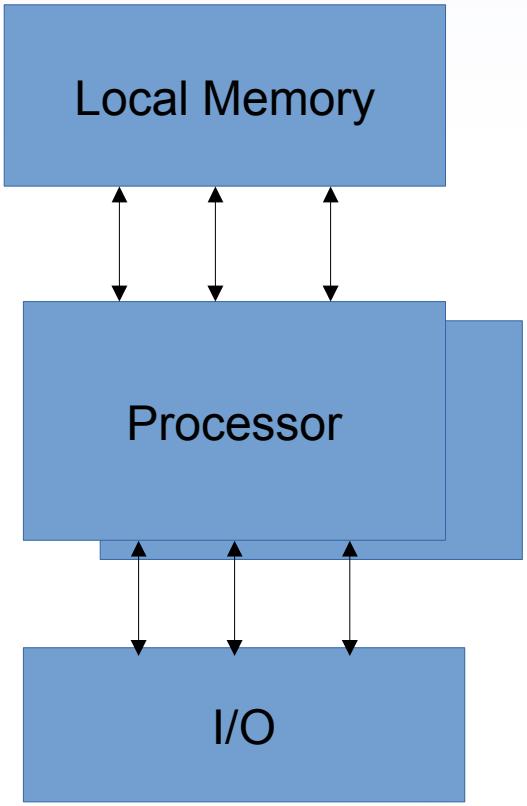

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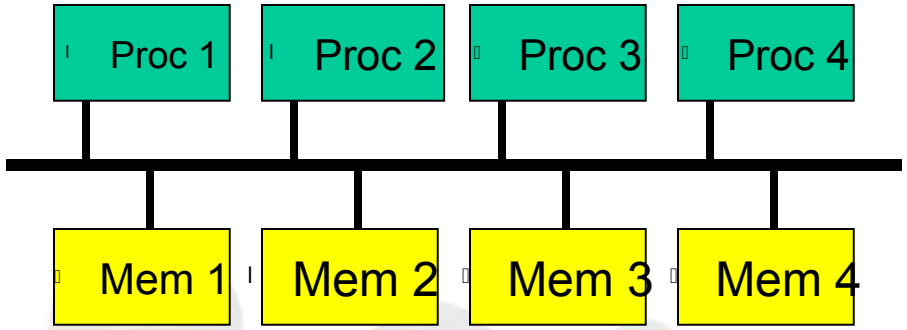
Symmetric Multiprocessors (SMP)

- A collection of processors, a collection of memory: both are connected through some interconnect (usually, the fastest possible)
- Symmetric because latency for any processor to access any memory is constant – uniform memory access (UMA)



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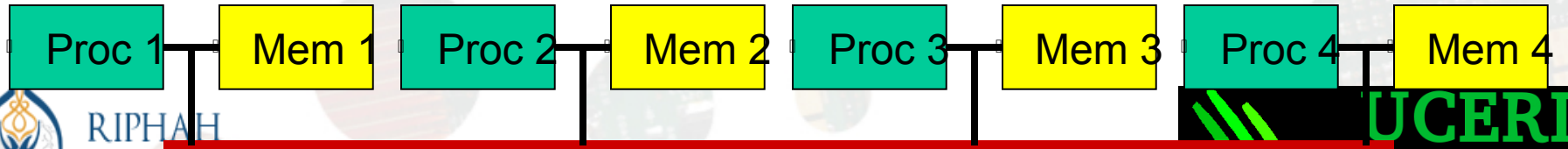
Distributed Memory Multiprocessors

- Each processor has local memory that is accessible through a fast interconnect
- The different nodes are connected as I/O devices with (potentially) slower interconnect
- Local memory access is a lot faster than remote memory – non-uniform memory access (NUMA)
- Advantage: can be built with commodity processors and many applications will perform well thanks to locality



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Shared Memory Architectures

- Key differentiating feature: the address space is shared, i.e., any processor can directly address any memory location and access them with load/store instructions

- Cooperation is similar to a bulletin board – a processor writes to a location and that location is visible to reads by other threads

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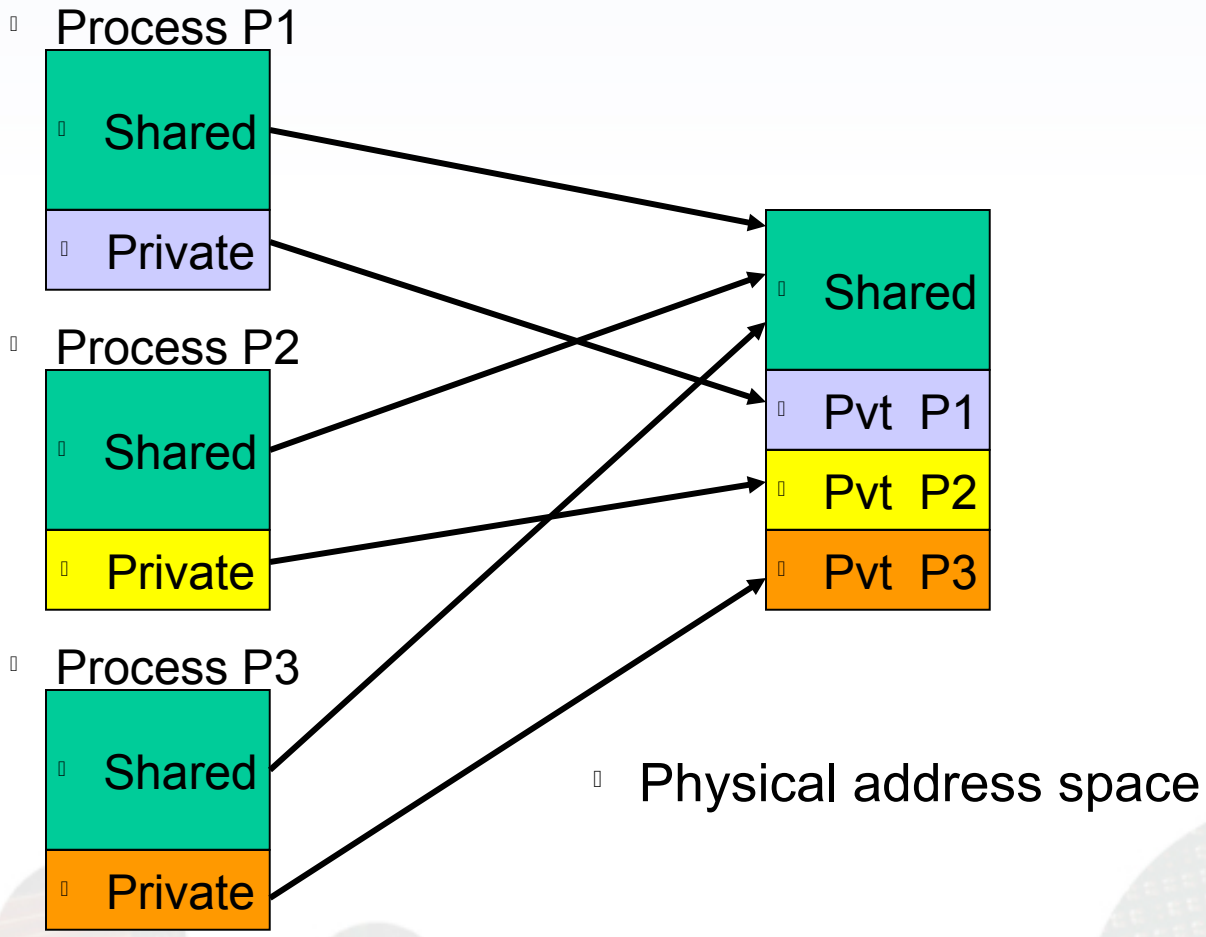
Shared Address Space



- Virtual address space of each process
- Physical address space

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Message Passing

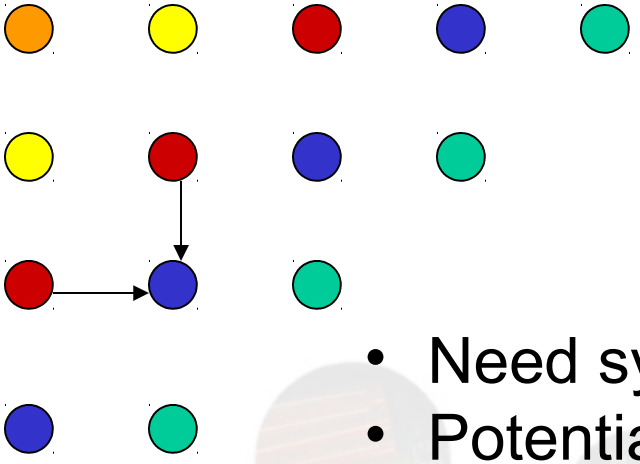
- Programming model that can apply to clusters of workstations, SMPs, and even a uniprocessor
- Sends and receives are used for effecting the data transfer – usually, each process ends up making a copy of data that is relevant to it
- Each process can only name local addresses, other processes, and a tag to help distinguish between multiple messages
- A send-receive match is a synchronization event – hence, we no longer need locks or barriers to co-ordinate

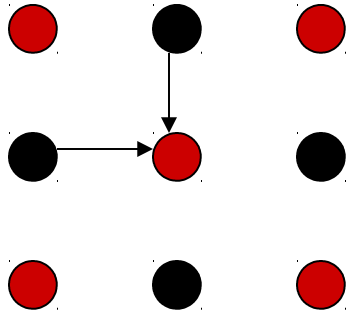
Models for SEND and RECEIVE

- Synchronous: SEND returns control back to the program only when the RECEIVE has completed
- Blocking Asynchronous: SEND returns control back to the program after the OS has copied the message into its space -- the program can now modify the sent data structure
- Nonblocking Asynchronous: SEND and RECEIVE return control immediately – the message will get copied at some point, so the process must overlap some other computation with the communication – other primitives are used to probe if the communication has finished or not

Deterministic Execution

- Shared-memory vs. message passing
- Function of the model for SEND-RECEIVE
- Function of the algorithm: diagonal, red-black ordering





- Need synch after every anti-diagonal
- Potential load imbalance

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Cache Coherence

A multiprocessor system is cache coherent if

- a value written by a processor is eventually visible to reads by other processors – write propagation

- two writes to the same location by two processors are seen in the same order by all processors – write serialization

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Cache Coherence Protocols

- Directory-based: A single location (directory) keeps track of the sharing status of a block of memory

- Snooping: Every cache block is accompanied by the sharing status of that block – all cache controllers monitor the shared bus so they can update the sharing status of the block, if necessary

➢ Write-invalidate: a processor gains exclusive access of a block before writing by invalidating all other copies
➢ Write-update: when a processor writes, it updates other shared copies of that block

Programming Models

- Facilitate system programmer to write
- code without going into detail of hardware
- Major Features:
  - Programmability
  - Portability
  - Scalability

- Automatically performs
  - Memory management
  - Scheduling
  - Synchronization