Delays
VLSI Design

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Activity

1) If the width of a transistor increases, the current will

increase decrease not change

2) If the length of a transistor increases, the current will

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3) If the supply voltage of a chip increases, the maximum transistor current will

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4) If the width of a transistor increases, its gate capacitance will

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6) If the supply voltage of a chip increases, the gate capacitance of each transistor will

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Topics

Combinational network delay.

Interconnect Delay

Clock Skew

Setup and Hold Time Violations

Optimization.

Combinational Network Delay

This delay occurs due to the propagation of signals through combinational logic elements such as logic gates. The delay depends on factors like gate delays, interconnect delays, and load capacitance.

Gate Sizing: Adjusting the sizes of gates to balance speed and power consumption.

Technology Mapping: Choosing appropriate logic cells to minimize delay.

Timing-Driven Synthesis: Synthesizing logic with timing constraints to optimize for performance.

Buffer Insertion: Adding buffers strategically to reduce signal propagation delays.

Clock Gating: Inserting logic to gate the clock signal to unused parts of the circuit, reducing power consumption and improving timing.

Interconnect Delay

This delay occurs due to the resistance, capacitance, and inductance of the wires connecting different components in the circuit. As wires become longer or narrower, their resistance and capacitance increase, leading to longer propagation delays.

Wire Sizing: Adjusting the width and spacing of wires to reduce resistance and capacitance.

Wire Length Reduction: Minimizing wire lengths by careful placement and routing.

Shielding and Twisting: Techniques to reduce noise and interference in long interconnects.

Segmentation: Breaking long wires into shorter segments to reduce delay.

Clock Distribution Techniques: Using specialized clock distribution networks to reduce clock skew and interconnect delay.

Clock Skew

This refers to the variation in arrival times of the clock signal at different parts of the circuit, leading to timing violations and reduced performance.

In practice, clock signals are often generated by a crystal oscillator, fed into a phase-locked loop (PLL), and distributed throughout the IC to each logic block and transistor within the system. One of the biggest challenges in this pursuit is known as clock skew, which can be defined as the difference between the clock signal arrival time of sequentially adjacent registers.

Clock Tree Synthesis: Designing clock distribution networks to minimize skew.

Clock Buffer Insertion: Adding buffers to equalize clock arrival times.

Clock Routing Optimization: Optimizing clock routing paths to reduce skew.

Global vs. Local Clocks: Using global and local clock domains strategically to minimize skew.

Clock Meshing: Using mesh-based clock distribution to reduce skew and improve reliability.

Setup and Hold Time Violations

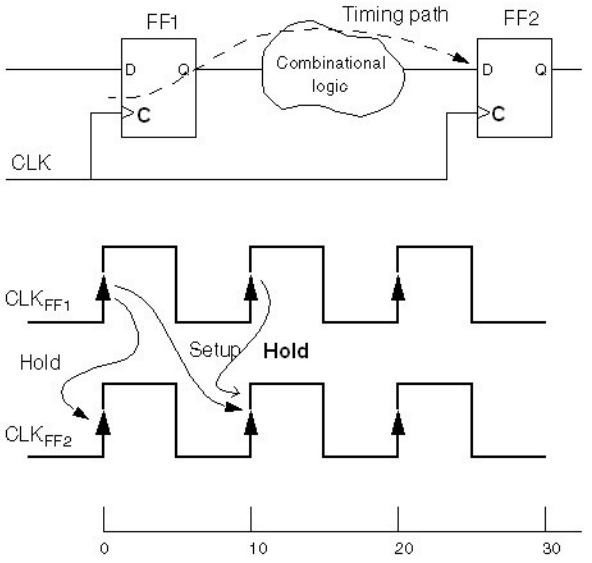
These occur when signals arrive too late or too early concerning the clock edge, causing incorrect data capture.

Static Timing Analysis (STA): Analyzing timing paths and constraints to identify and address violations.

Clock Domain Crossing (CDC) Analysis: Ensuring proper synchronization between different clock domains.

Delay Budgeting: Allocating timing margins to accommodate variations and reduce violations.

Constraint Optimization: Fine-tuning timing constraints to meet setup and hold time requirements.



Sources of delay

- Gate delay
- Drive Load
- Lumped Load
- Wire
- Transmission Line

Gate Delay: This delay occurs within the logic gates themselves as signals propagate through the transistors and other components that make up the gate. Gate delay is influenced by factors like transistor sizing, transistor type (e.g., NMOS, PMOS), and manufacturing process variations.

Drive Load Delay: Drive load delay refers to the delay caused by driving the output signal onto the interconnect or to other gates. This delay depends on the output impedance of the driving gate and the capacitance of the load it is driving.

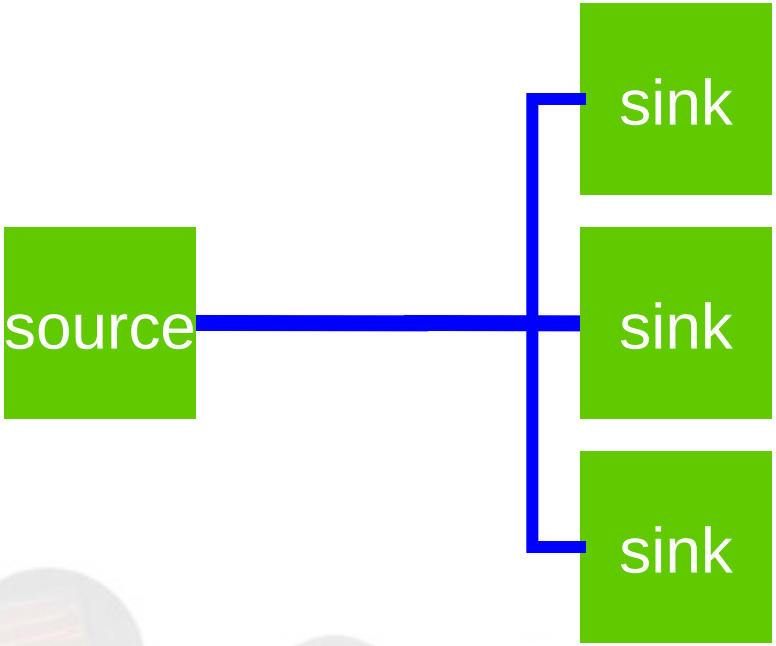
Lumped Load Delay: Lumped load delay is similar to drive load delay but occurs when the load capacitance is concentrated at a single point rather than distributed along the interconnect. It's common in cases where multiple gates are connected to a single node.

Wire Delay: Wire delay is the delay caused by the interconnect wires connecting different components in the circuit. It is influenced by factors such as wire length, wire width, wire resistance, wire capacitance, and the dielectric material between wires.

Transmission Line Delay: Transmission line delay occurs when the interconnect behaves like a transmission line due to its length and electrical properties. This type of delay becomes significant when the interconnect length approaches a significant fraction of the signal wavelength. Transmission line effects include phenomena like signal reflections, impedance mismatch, and signal attenuation.

Fanout

Fanout adds capacitance.

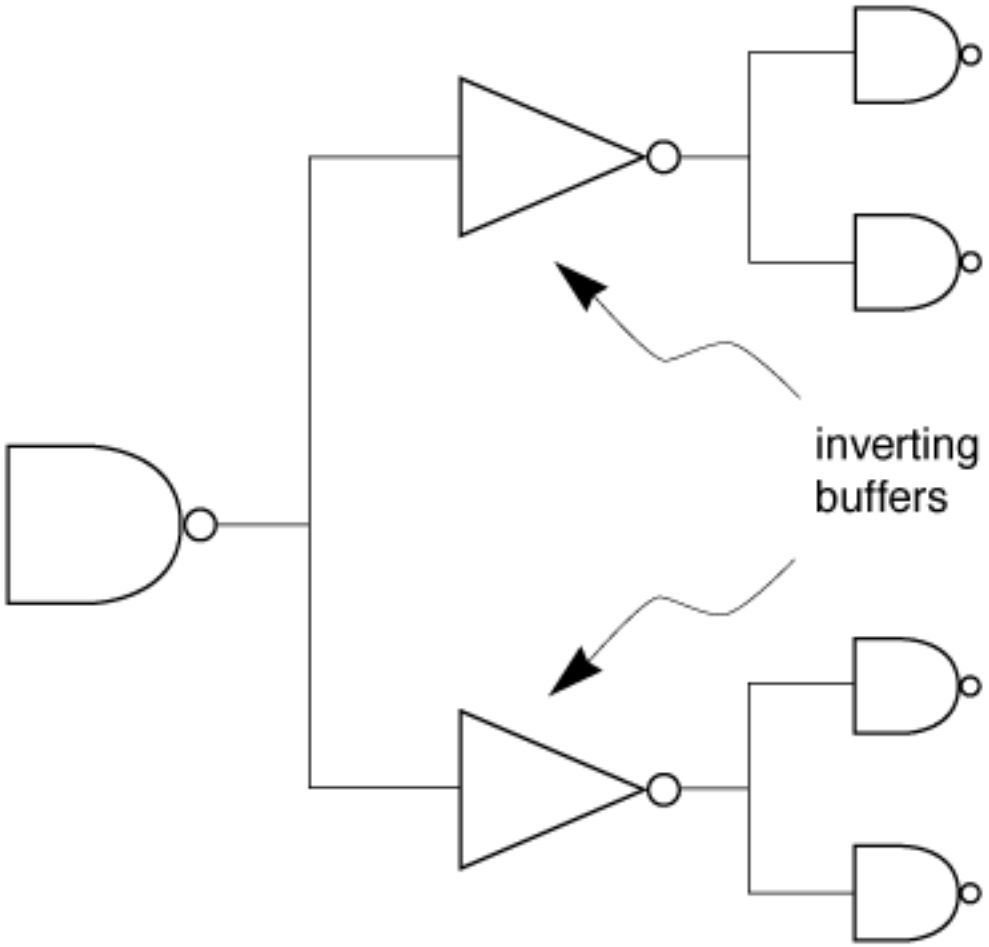


Ways to drive large fanout

Increase sizes of driver transistors. Must take into account rules for driving large loads.

Add intermediate buffers. This may require/allow restructuring of the logic.

Buffers

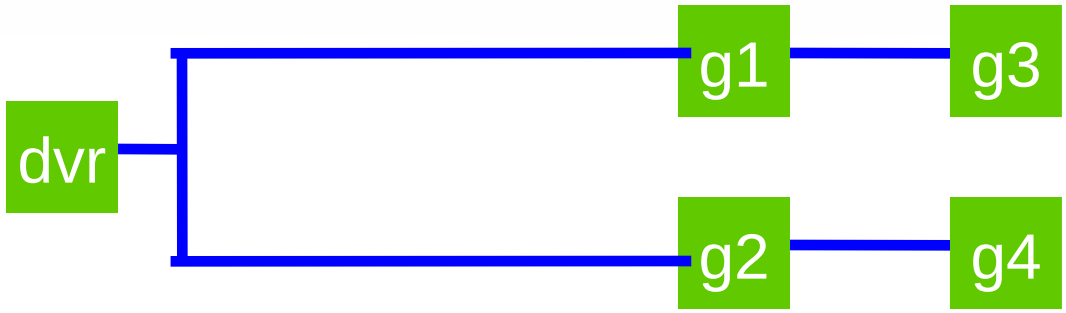


Wire capacitance

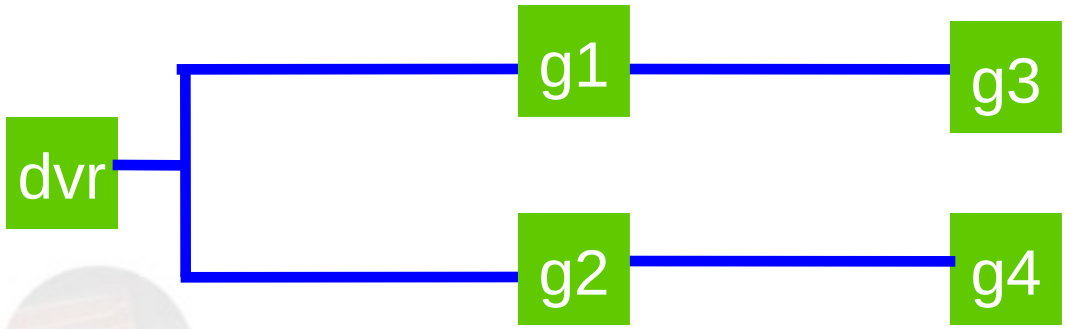
Use layers with lower capacitance.

Redesign layout to reduce length of wires with excessive delay.

Placement and wire capacitance



unbalanced load



more balanced

Path delay

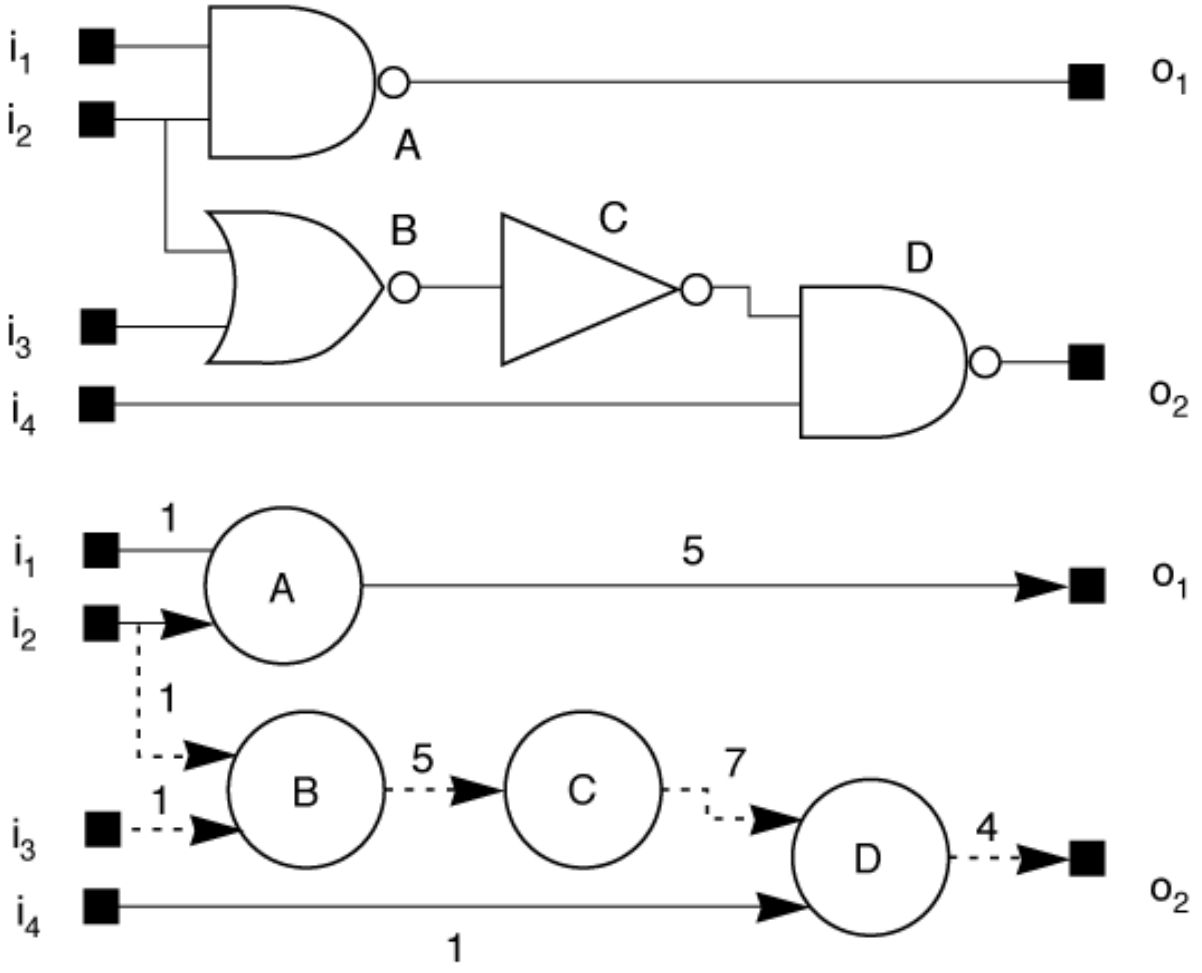
Combinational network delay is measured over paths through network.

Can trace a causality chain from inputs to worst-case output.

Path delay example

network

graph model



Critical path

Critical path = path which creates longest delay.

Can trace transitions which cause delays that are elements of the critical delay path.

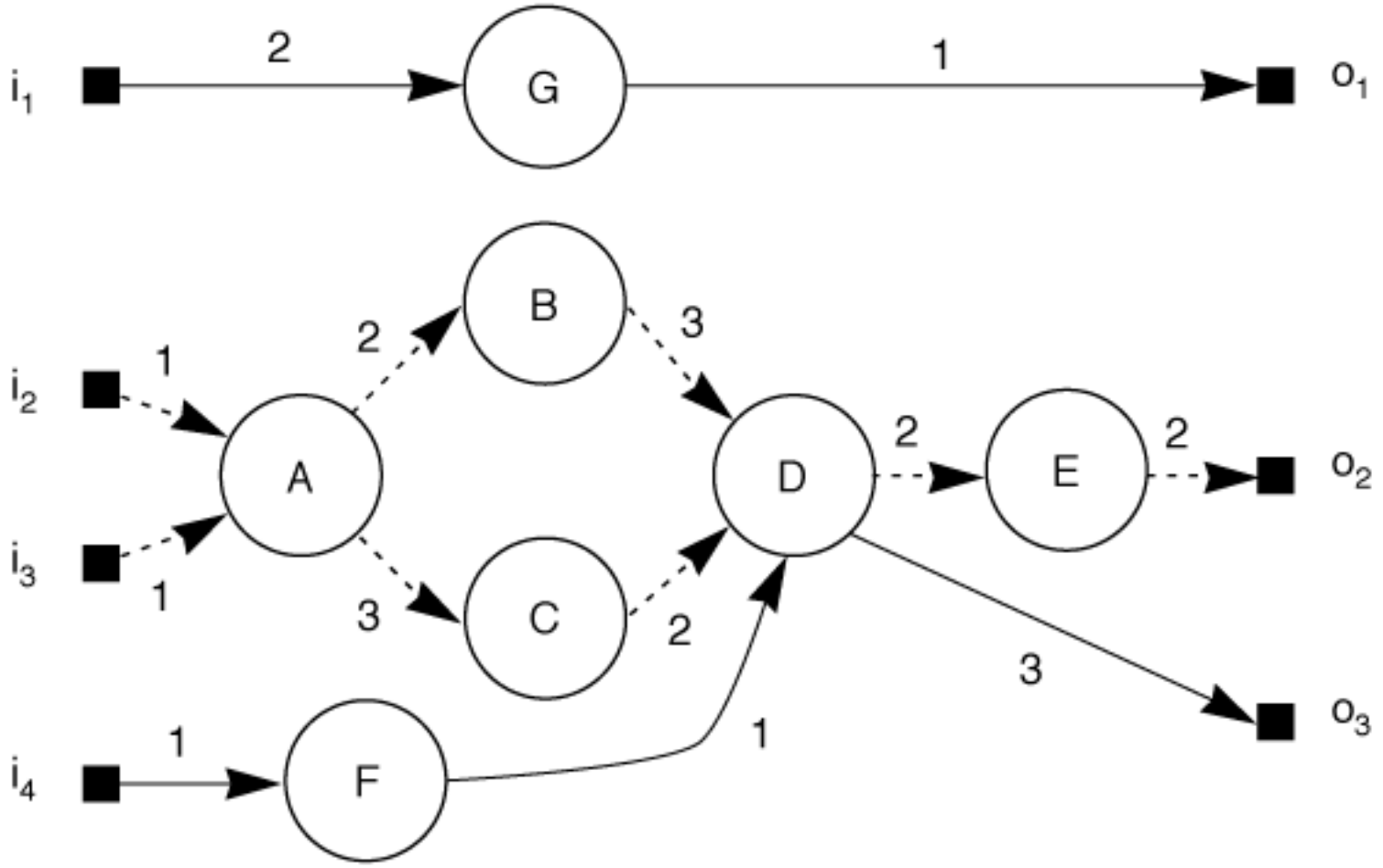
Delay model

Nodes represent gates.

Assign delays to edges—signal may have different delay to different sinks.

Lump gate and wire delay into a single value.

Critical path through delay graph



Reducing critical path length

To reduce circuit delay, must speed up the critical path—reducing delay off the path doesn’t help.

There may be more than one path of the same delay. Must speed up all equivalent paths to speed up circuit.

Must speed up cut-set through critical path.

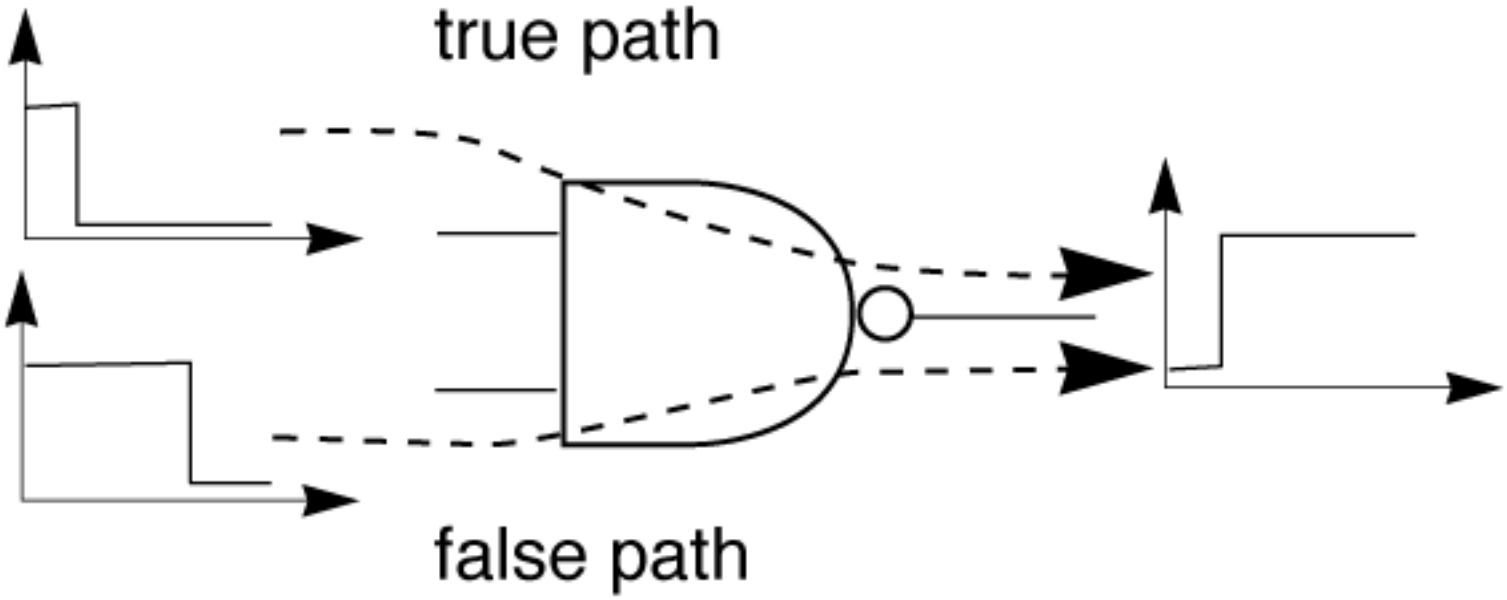
False paths

Logic gates are not simple nodes—some input changes don’t cause output changes.

A false path is a path which cannot be exercised due to Boolean gate conditions.

False paths cause pessimistic delay estimates.

False path example



Logic optimization

Logic synthesis programs transform Boolean expressions into logic gate networks in a particular library.

Optimization goals: minimize area, meet delay constraint.

Logic transformations

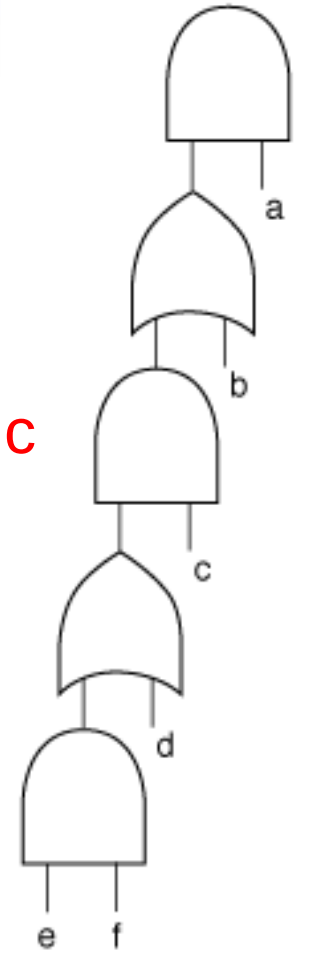
Can rewrite by using subexpressions.

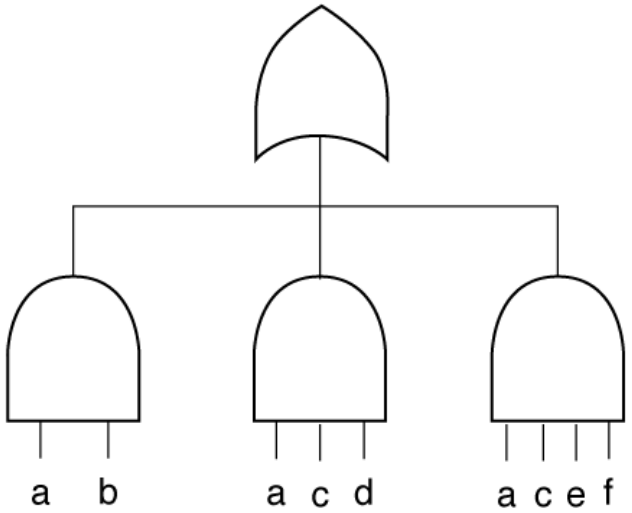
Flattening logic increases gate fan-in.

Logic rewrites may affect gate placement.

Logic rewrites

deep logic





shallow logic

Technology-independent optimizations

Works on Boolean expression equivalence.

Estimates size based on number of literals.

Uses factorization, re-substitution, minimization, etc. to optimize logic.

Technology-independent phase uses simple delay models.

Technology-dependent optimizations

Maps Boolean expressions into a particular cell library.

Mapping may take into account area, delay.

May perform some optimizations in addition to simple mapping.

Allows more accurate delay models.

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