Namal University Mianwali
Department of Electrical Engineering

COURSE OUTLINE – Spring

1. COURSE DETAILS

Title:	VLSI Design
Code:	EE-473
Credit(s):	3 Credit Hours (3Hrs Theory and 1 Hrs Lab/Project Work)
Pre-requisite(s):	Digital System Design
Co-requisite(s):	None

2. INSTRUCTOR DETAILS

Name:	Tassadaq Hussain
Lecture Timings:	Wednesday 9:30 pm to 11:00 pm & Friday 3:00 pm to 4:30 pm
Office Location:	Faculty Office 17
Office Telephone:	120
Office Hours:	Monday - Friday 9am-1pm
E-mail:	Tassadaq.hussain@namal.edu.pk

3. COURSE RELEVANT DETAILS

Course Description:

Introduction to integrated circuits, IC fabrication, monolithic integrated circuits, introduction to MOS technology, basic electrical properties of MOS and BiCMOS circuits, basic digital building blocks using MOS transistor basic circuit concepts, ultra-fast VLSI circuits and systems and their design.

Course Learning Outcomes (CLOs)

On successful completion of this course, the student will be able to:

Course Learning Outcome	CLO Statement	Taxonomy Level
CLO-1	Identify the Physical Layout and Gate Level	C1(Cognitive)

	System Design using 65 nm ASIC technology.	
CLO-2	Discuss a Gate Array, Full Custom, Structure and Standard ASICs. Understand ASIC technologies with respect to cost, performance and flexibility.	C2(Cognitive)
CLO-3	Analyze the ASIC chip while targeting trade-off such as energy, power and area	C4(Cognitive)

Program Learning Outcomes (PLO's):

PLO-2. Problem Analysis

An ability to identify, formulate, research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences engineering sciences.

PLO-3. Design/Development of Solutions

An ability to design solutions for complex engineering problems and design systems, components or processes that meet specified needs with appropriate consideration for public health and safety, cultural, societal, and environmental considerations.

PLO-5: Modern Tool Usage:

An ability to create, select and apply appropriate techniques, resources, and modern engineering and IT tools, including prediction and modeling, to complex engineering activities, with an understanding of the limitations.

MAPPING OF CLOs TO PROGRAM LEARNING OUTCOMES

CLOs/PLOs	CLO:1	CLO:2	CLO:3
PLO:2 (**Problem Analysis**)	✓		
PLO:3 (**Design/Development of Solutions)**		✓	
PLO:5 (**Modern Tool Usage)**			✓

Week#	**Topics Covered in Class**	**Reference in Book/ Course Material**	**Course Assessments**
			Assignment/ Test/Project/Lab Report/Quiz
Week 1	Past Present and Future of Integrated Circuits	CMOS VLSI Design	
Week 2	Introduction to VLSI Classification of ICs Design Flow (Y-Map) Fabrication Process	CMOS VLSI Design	Quiz #1
Week 3	VLSI Components and Architectures (I) Bipolar Technologies MOS Transistor Theory	CMOS VLSI Design	
Week 4	VLSI Components and Architectures (II) Delays, Time, Area, Speed, Power (static , dynamic power)	CMOS VLSI Design	Assignment # 1
Week 5	Types of ASIC ASIC and FPGA VLSI: ASIC Design Flow: • Chip Specification • Design Entry / Functional Verification, • RTL block synthesis / RTL Function, • Chip Partitioning, • Design for Test (DFT) Insertion • Floor Planning (blueprint your chip), • Placement, • Clock tree synthesis, • Routing, • Final Verification (Physical Verification and Timing), • GDS II – Graphical Data Stream Information Interchange	VLSI Physical Design: From Graph Partitioning to Timing Closure	
Week 6	Switch/Transistor Level Circuit Design (I): MOS, NMOS, PMOS, CMOS	VLSI Physical Design:	
Week 7	Gate Level Design Computational Logic Circuits: HDL and Layout Design	VLSI Physical Design:	Quiz # 2
Week 8	Basic Components of Digital System Memories (SRAMs, DRAMs), Microprocessors, Buses	Digital VLSI Design and Simulation with Verilog	
Mid Term			

Week 9	Design For Test Testing, Simulating and Prototyping	Digital VLSI Design and Simulation with Verilog	Quiz # 3
Week 10	Abstract Level Design Components: ALU, Buses, Registers etc.	Digital VLSI Design and Simulation with Verilog	Assignment # 2
Week 11	RISC-V based System on Chip Design	Digital VLSI Design and Simulation with Verilog	
Week 12	Processor Design Analysis		Quiz#04
Week 13	Processor based System Design I		
Week 14	Processor based System Design II		
Week 15			
Week 16	Revision		
	End Term		

4. TEACHING METHODOLOGY

Active learning through lecturing, and tutorials, when required

Project-Based Learning.

Assignment , Quiz, Related videos from YouTube

5. TEACHING MATERIAL

Text Books

1. CMOS VLSI Design_ A Circuits and Systems Perspective (4th Edition 2010)
2. A Practical Approach to VLSI System on Chip (SoC) Design. A Comprehensive Guide
3. VLSI Physical Design: From Graph Partitioning to Timing Closure.

CMOS VLSI Design

6. ONLINE RESOURCES

Open-source Tools

https://vlsiresources.com/opensourcevlsi/

https://opencores.org/

7. COURSE ASSESSMENT AND EVALUATION

The student's performance will be assessed through a number of assessment instruments. The table below displays the appropriate distribution of grade weights and their corresponding linkage with the stated CLOs.

No	Assessments Instruments		Grade Weight	Course Learning Outcomes		
			%	1	2	3
1	**Continuous Assessments (60%)**	Assignment 1	2.5	✔		
2		Assignment 2	2.5		✔	
3		Quiz 1	2.5	✔		
4		Quiz 2	2.5		✔	
5		Quiz 3	2.5		✔	
6		Quiz 4	2.5			✔

	7		Midterm	30	✔	✔	
	8		CEP	15	✔	✔	✔
	9	**Final Examination (40)**		50		✔	✔

8. UNIVERSITY POLICIES

The students are required to fully understand and observe the following policies of the university. Seventy five percent (75%) attendance is mandatory for the lectures/laboratory work delivered in the course. For further details, please refer to university policies mentioned in student handbook and undergraduate academic regulations of Namal University Mianwali.

9. VERIFICATION

(i) I verify that the content of this document are correct and up-to-date.

Dr.Tassadaq Hussain **Instructor's Name and Signature**	_____ **Date**

(ii) I have reviewed course-outline and state that it complies with Namal University policies and guidelines.

Dr. Sajjad ur Rehman **Name and Signature of Head of Department**	_____ **Date**